

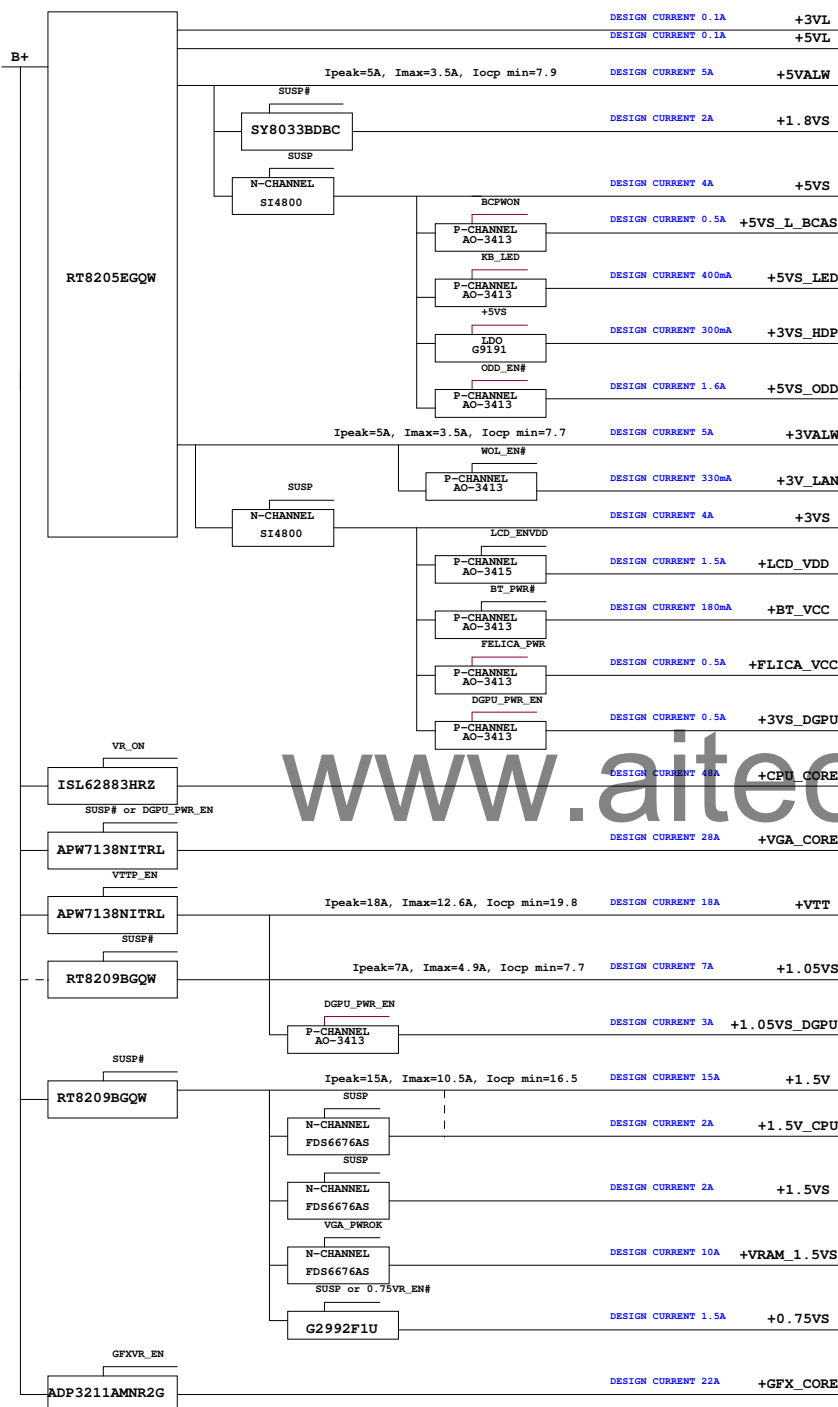
PHQAA

Marseille 10R/10RG

LA-6831P REV 0.1 Schematic

Intel Processor (Sandy Bridge) / PCH (Cougar Point)
2010-07-05 Rev 0.1

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				Size	Document Number	Rev
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Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	Power Tree	
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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane \ State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b
Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9A H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	Light Sensor	52 H	0101 0010 b

Platform	SKU	CPU	PCH	VGA
Calpella	UMA (OPT@)	Arrandale	HM55@/HM57@	N/A
	Discrete (DIS@)	Clarksfield/Arrandale	HM55@/HM57@/PM55@	N11P@/N11M@
	Optimus (OPT@)	Arrandale	HM55@/HM57@	N11P@/N11M@

BTO Option Table

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	MDC@	CIR@	KBL@

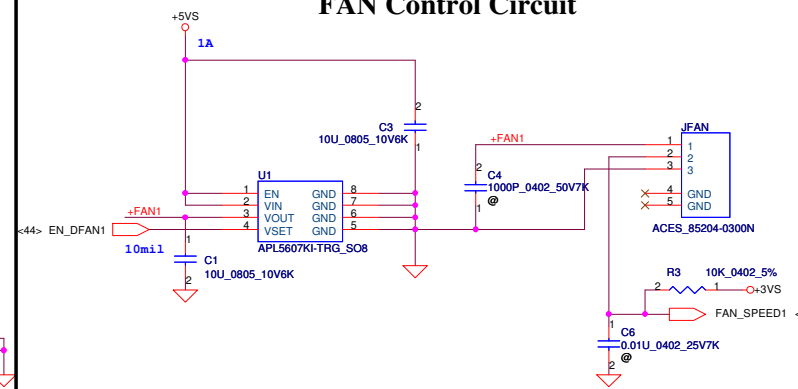
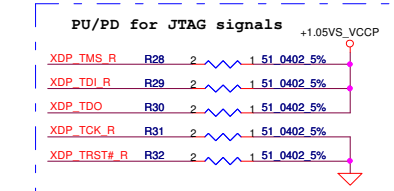
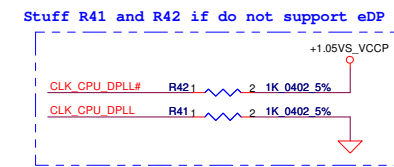
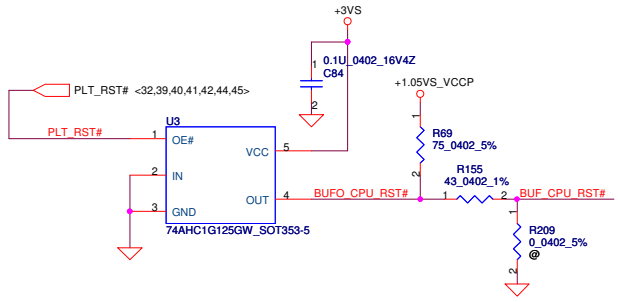
Function	Felica	BLUE TOOTH	G-SENSOR	SKU		LVDS		Camera & Mic	
description	Felica	BLUE TOOTH	G-SENSOR	SKU		3D Panel		Camera & Mic	
explain	Felica	BLUE TOOTH	G-SENSOR	Discrete	Optimus	Discrete		Optimus	Camera & Mic
BTO	FELICA@	BT@	GSENSOR@	DIS@	OPT@	3D@	NO3D@	OPTFH@	CAM@

Function	S3 Power Saving		GPU					
description	S3 Power Saving		N11P & N11E			N11M		
explain	No Power Saving	Power Saving	VRAM	N11P	N11E	N11M-GE1	N11M-GE2	N11M-OP1
BTO	NOPS@	PS@	8PCS@	N11P@	N11E@	N11MGE1@	N11MGE2@	N11MOP@

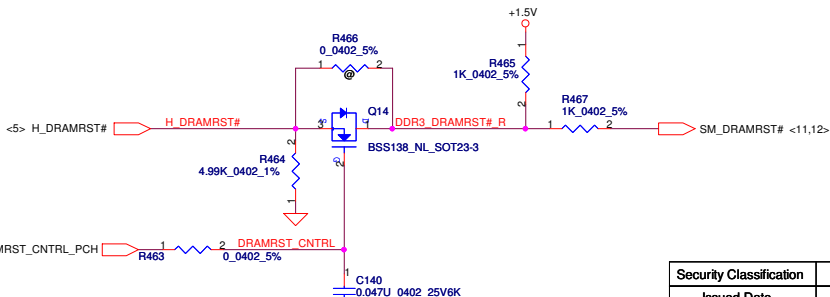
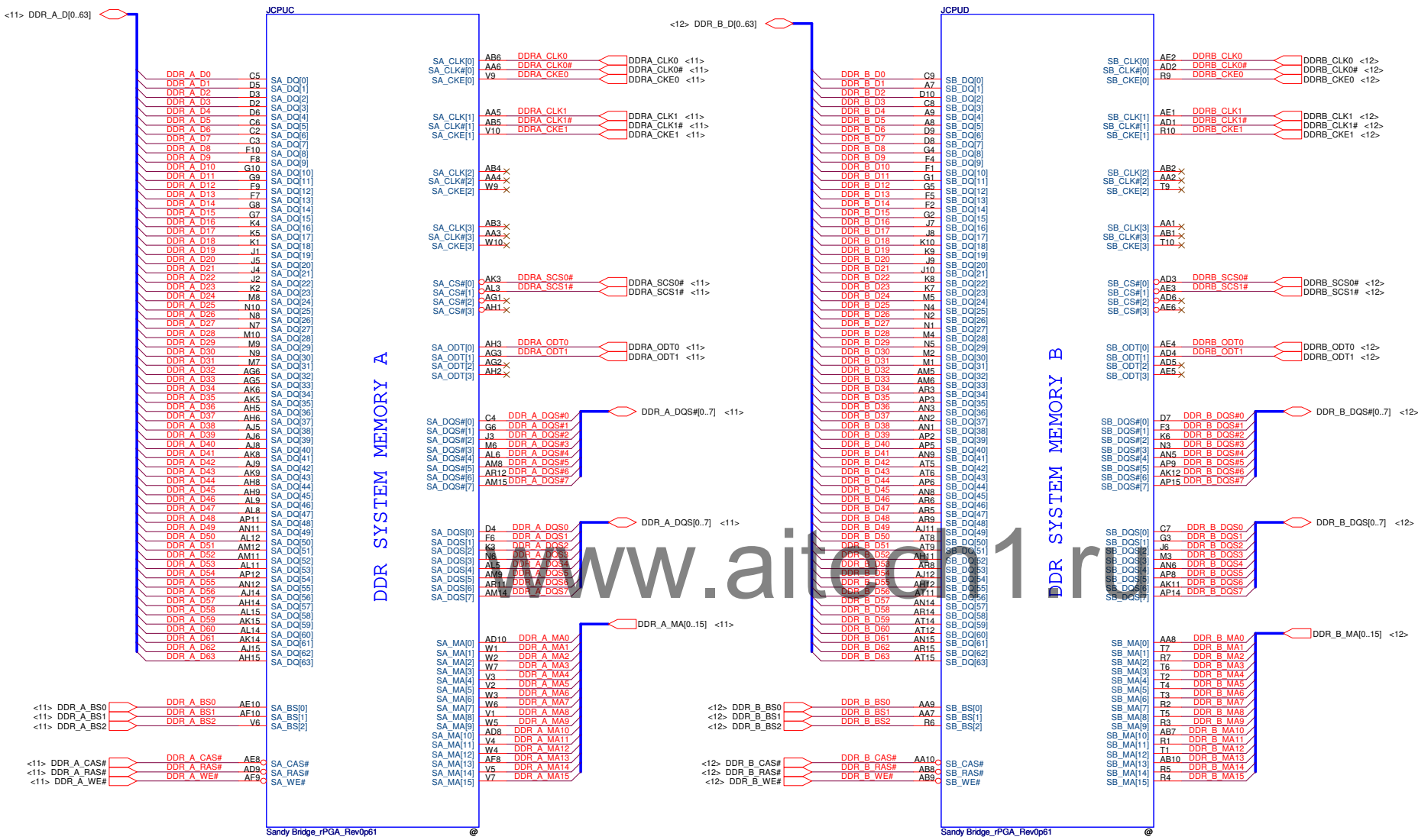
Function	Card reader		New Card
description	JMB385C/389C		New Card
explain	JMB385C	JMB389C	New Card
BTO	JMB385@	JMB389@	NEW@

STATE	SIGNAL		
	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

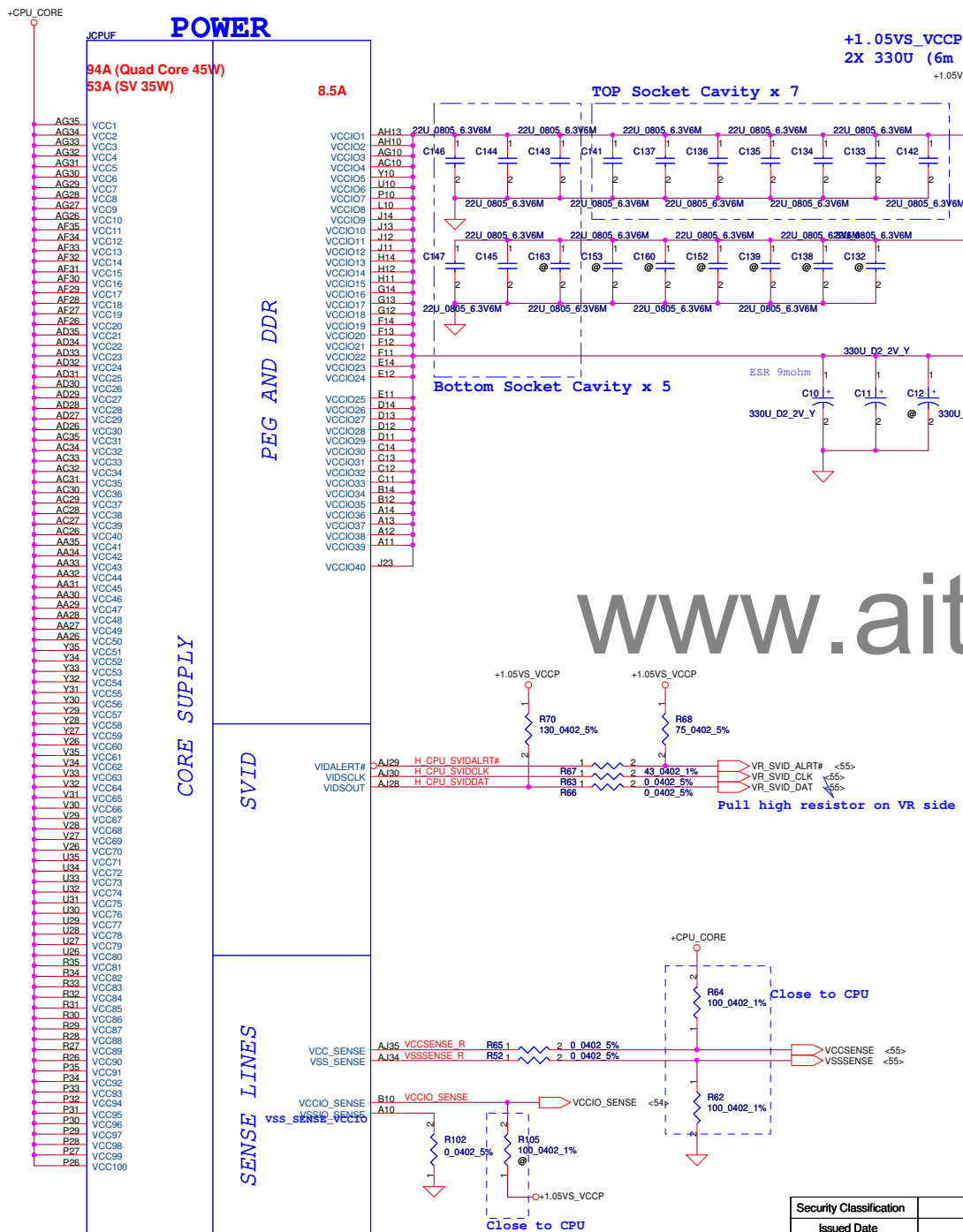
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Issued Date	200910/9	Deciphered Date	2010/01/23	Notes List		
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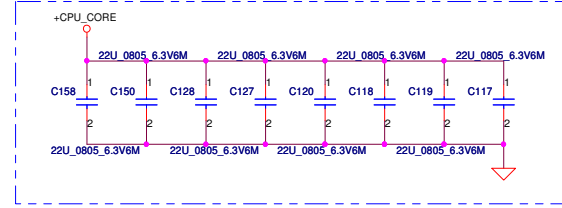
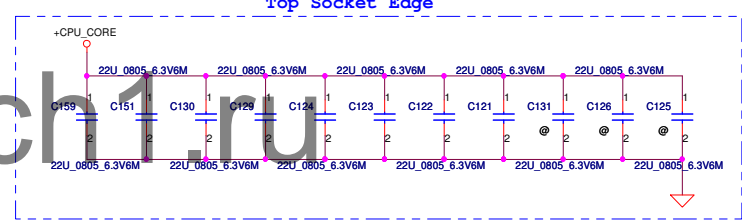
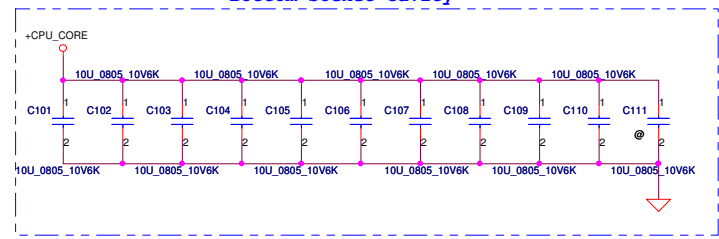
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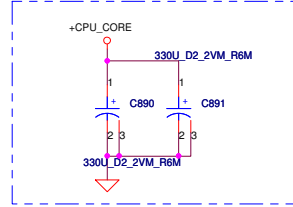
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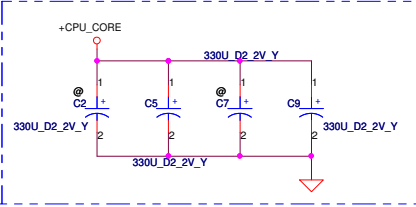
+CPU_CORE Decoupling:
4X 470U (4m ohm), 16X 22U, 10X 10U



Co-Lay with C2, C5, C7, C9



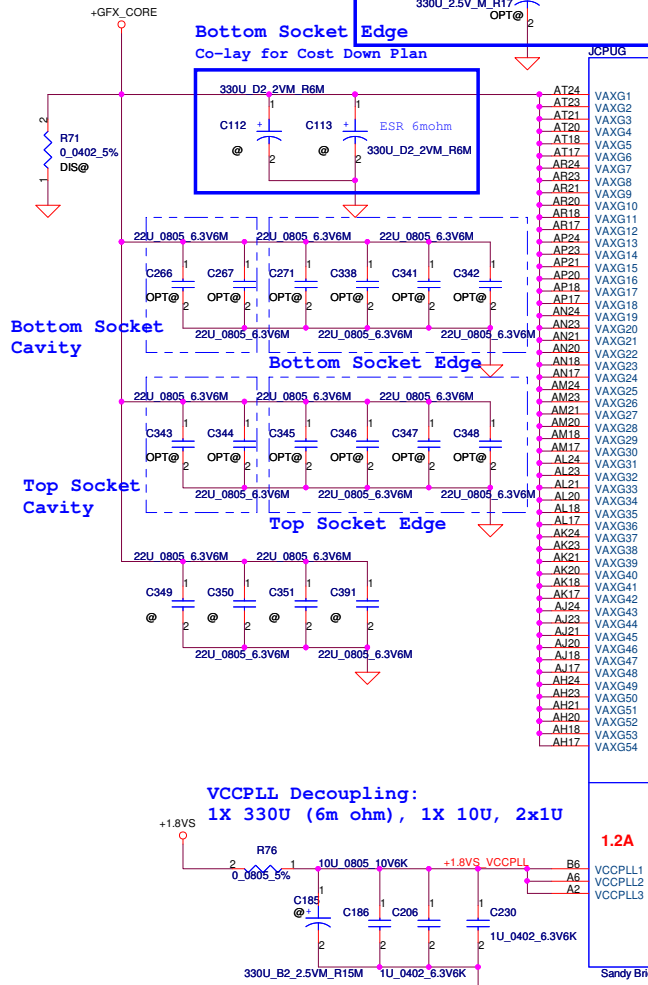
Bottom Socket Edge



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+GFX_CORE Decoupling:
2X 470U (4m ohm), 12X 22U



POWER

SENSE LINES
VREF
VSSAXG_SENSE

5A
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VDDQ9
VDDQ10
VDDQ11
VDDQ12
VDDQ13
VDDQ14
VDDQ15

6A
VCCSA1
VCCSA2
VCCSA3
VCCSA4
VCCSA5
VCCSA6
VCCSA7
VCCSA8

1.8V RAIL
VCCPLL1
VCCPLL2
VCCPLL3

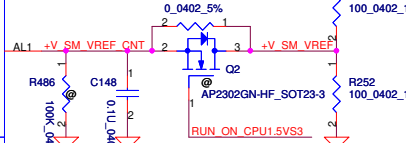
1.2A
VCCSA_SENSE
VCCSA_VID0
VCCSA_VID1

33A
VAXG1
VAXG2
VAXG3
VAXG4
VAXG5
VAXG6
VAXG7
VAXG8
VAXG9
VAXG10
VAXG11
VAXG12
VAXG13
VAXG14
VAXG15
VAXG16
VAXG17
VAXG18
VAXG19
VAXG20
VAXG21
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VAXG54

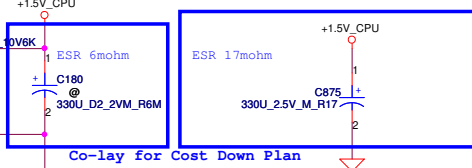
DDR3 -1.5V RAILS

MISC
VCCSA_SENSE
VCCSA_VID0
VCCSA_VID1

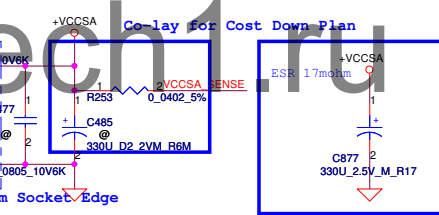
+V_SM_VREF should
have 20 mil trace width



+1.5V_CPU Decoupling:
1X 330U (6m ohm), 6X 10U



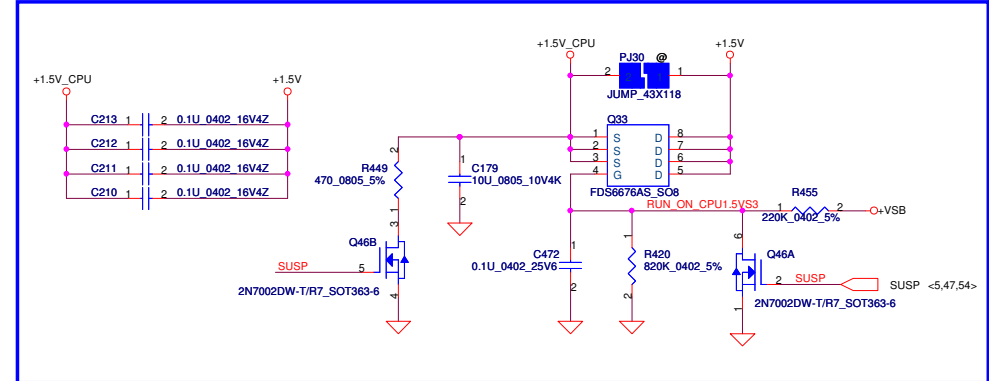
+VCCSA Decoupling:
1X 330U (6m ohm), 3X 10U

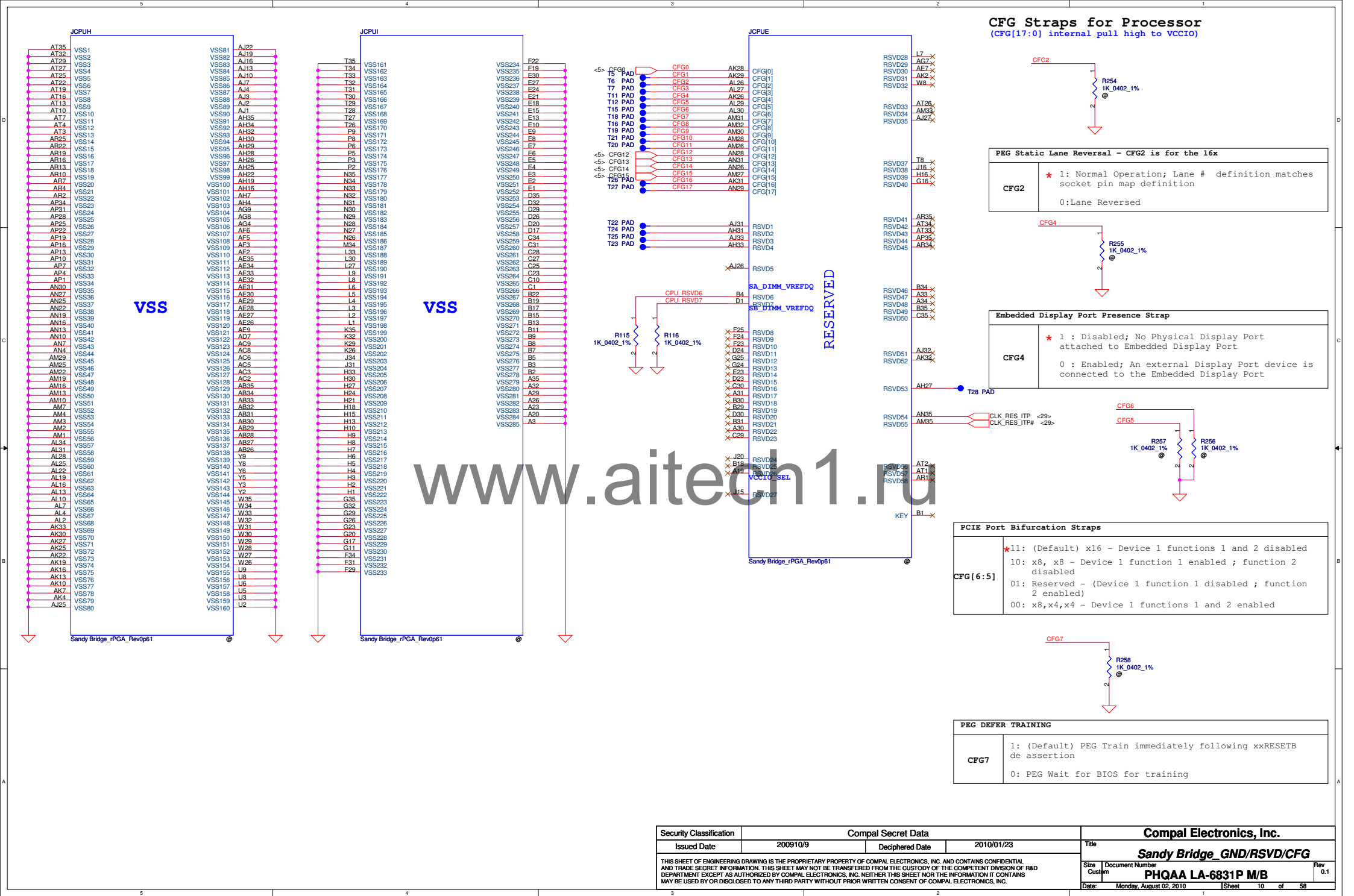


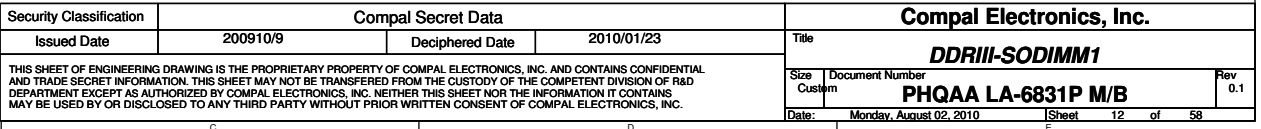
VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.75 V
1	1	0.65 V

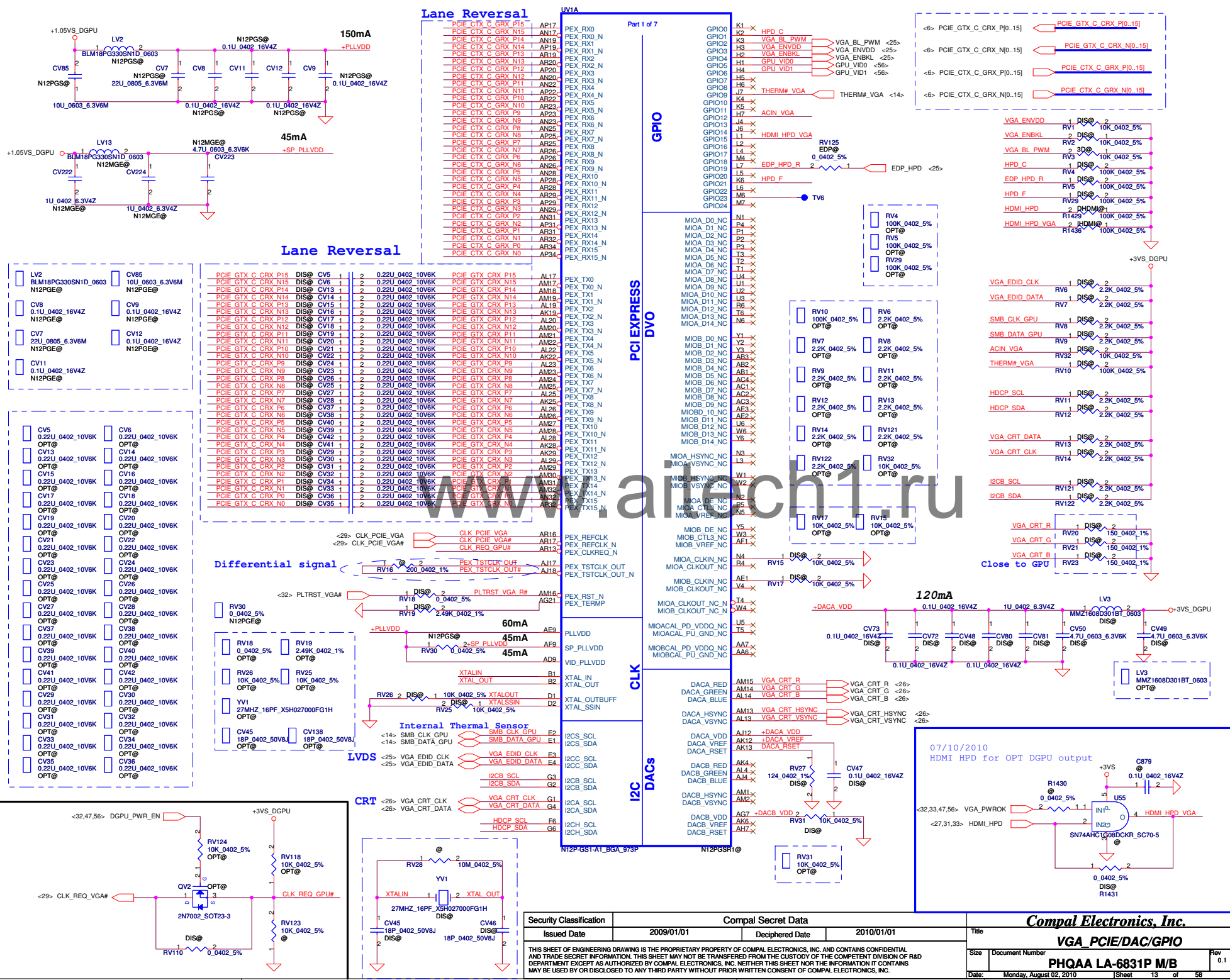
For Sandy Bridge

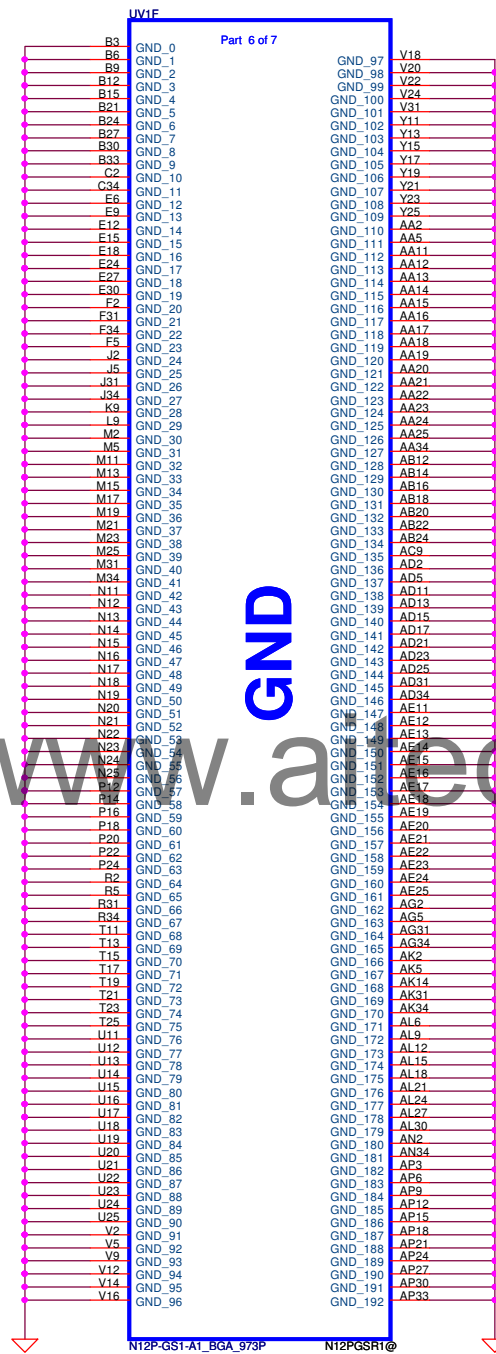
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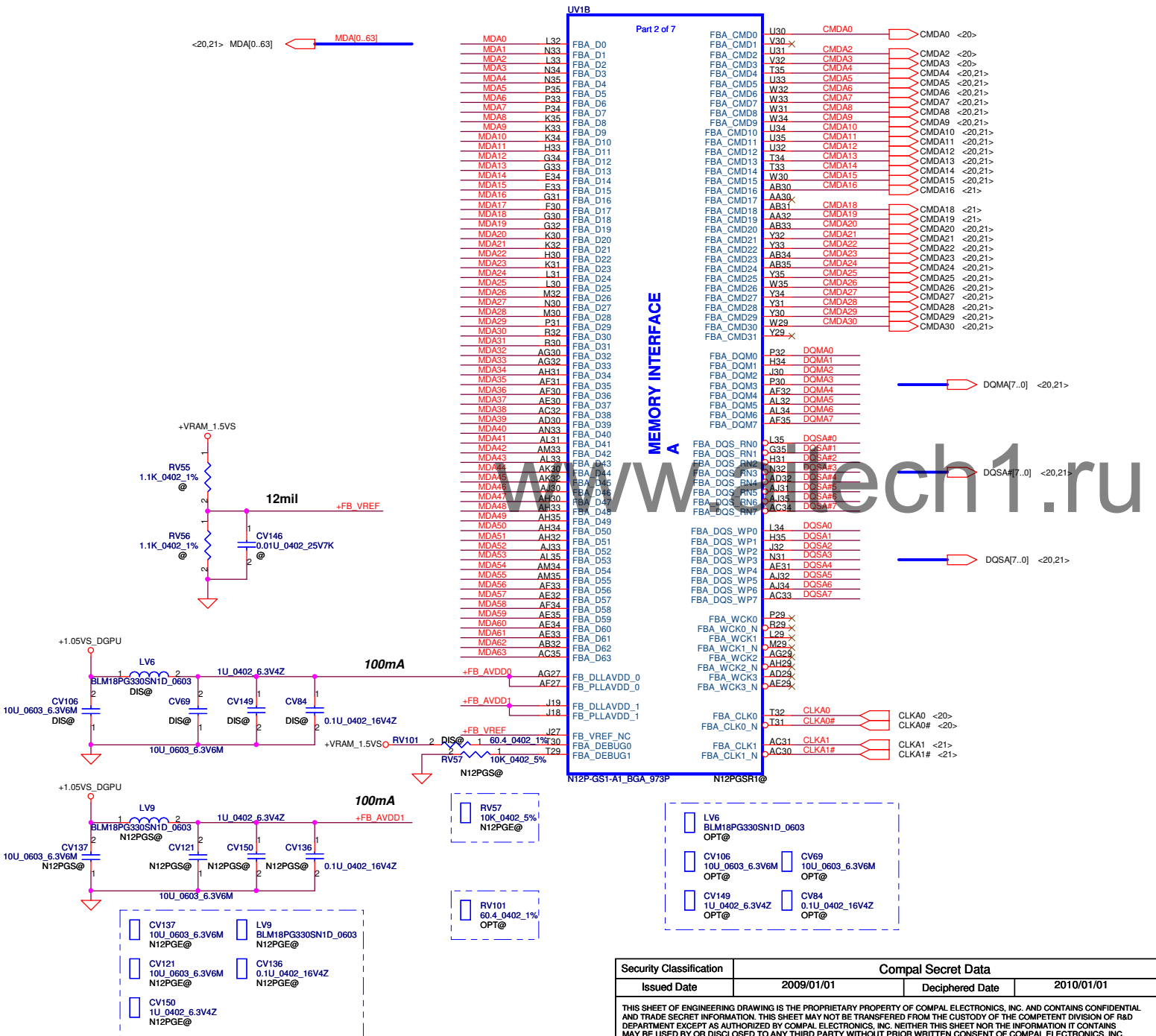








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GB2-128 Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19	ODT_H	
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

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Compal Electronics, Inc.			
Title VGA_MEM Interface A			
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<22,23> MDB[0..63]

MDB[0..63]

MDB0 B13 FBC_D0
MDB1 D13 FBC_D1
MDB2 A13 FBC_D2
MDB3 C16 FBC_D3
MDB4 B16 FBC_D4
MDB5 A17 FBC_D5
MDB6 D16 FBC_D6
MDB7 C13 FBC_D7
MDB8 B11 FBC_D8
MDB9 C11 FBC_D9
MDB10 A11 FBC_D10
MDB11 C10 FBC_D11
MDB12 B8 FBC_D12
MDB13 A8 FBC_D13
MDB14 B8 FBC_D14
MDB15 A8 FBC_D15
MDB16 E8 FBC_D16
MDB17 F8 FBC_D17
MDB18 E9 FBC_D18
MDB19 F9 FBC_D19
MDB20 D8 FBC_D20
MDB21 D11 FBC_D21
MDB22 E11 FBC_D22
MDB23 D12 FBC_D23
MDB24 E13 FBC_D24
MDB25 F13 FBC_D25
MDB26 F14 FBC_D26
MDB27 F15 FBC_D27
MDB28 E16 FBC_D28
MDB29 F16 FBC_D29
MDB30 F17 FBC_D30
MDB31 D29 FBC_D31
MDB32 D27 FBC_D32
MDB33 F28 FBC_D33
MDB34 E28 FBC_D34
MDB35 D26 FBC_D35
MDB36 F25 FBC_D36
MDB37 D24 FBC_D37
MDB38 E25 FBC_D38
MDB39 F23 FBC_D39
MDB40 E32 FBC_D40
MDB41 D33 FBC_D41
MDB42 E31 FBC_D42
MDB43 C33 FBC_D43
MDB44 F29 FBC_D44
MDB45 D30 FBC_D45
MDB46 E29 FBC_D46
MDB47 D29 FBC_D47
MDB48 E29 FBC_D48
MDB49 C31 FBC_D49
MDB50 B31 FBC_D50
MDB51 C32 FBC_D51
MDB52 B32 FBC_D52
MDB53 B35 FBC_D53
MDB54 B34 FBC_D54
MDB55 A29 FBC_D55
MDB56 B28 FBC_D56
MDB57 A28 FBC_D57
MDB58 C28 FBC_D58
MDB59 C26 FBC_D59
MDB60 D25 FBC_D60
MDB61 B25 FBC_D61
MDB62 A25 FBC_D62
MDB63

UVIC

Part 3 of 7

MEMORY INTERFACE C

FBC_CMD0 F18 CMDB0
FBC_CMD1 E19 CMDB2
FBC_CMD2 D18 CMDB3
FBC_CMD3 C17 CMDB4
FBC_CMD4 F19 CMDB5
FBC_CMD5 B17 CMDB6
FBC_CMD6 E20 CMDB7
FBC_CMD7 B19 CMDB8
FBC_CMD8 D20 CMDB9
FBC_CMD9 A19 CMDB10
FBC_CMD10 C19 CMDB11
FBC_CMD11 F20 CMDB12
FBC_CMD12 B20 CMDB13
FBC_CMD13 G21 CMDB14
FBC_CMD14 F22 CMDB15
FBC_CMD15 F24 CMDB16
FBC_CMD16 E23 CMDB18
FBC_CMD17 C25 CMDB19
FBC_CMD18 F21 CMDB20
FBC_CMD19 E22 CMDB21
FBC_CMD20 D21 CMDB22
FBC_CMD21 A23 CMDB23
FBC_CMD22 D22 CMDB24
FBC_CMD23 B23 CMDB25
FBC_CMD24 C22 CMDB26
FBC_CMD25 B22 CMDB27
FBC_CMD26 A22 CMDB28
FBC_CMD27 A20 CMDB29
FBC_CMD28 G20 CMDB30
FBC_CMD29
FBC_CMD30
FBC_CMD31

FBC_QM0 A16 DQMB0
FBC_QM1 E11 DQMB1
FBC_QM2 D15 DQMB2
FBC_QM3 D27 DQMB3
FBC_QM4 D34 DQMB4
FBC_QM5 A34 DQMB5
FBC_QM6 D28 DQMB6
FBC_QM7

FBC_QS_RN0 B14 DQSB#0
FBC_QS_RN1 C10 DQSB#1
FBC_QS_RN2 E14 DQSB#2
FBC_QS_RN3 F26 DQSB#3
FBC_QS_RN4 D31 DQSB#4
FBC_QS_RN5 A31 DQSB#5
FBC_QS_RN6 A26 DQSB#6
FBC_QS_RN7

FBC_QS_WP0 C14 DQSB#0
FBC_QS_WP1 A10 DQSB#1
FBC_QS_WP2 E10 DQSB#2
FBC_QS_WP3 D14 DQSB#3
FBC_QS_WP4 E26 DQSB#4
FBC_QS_WP5 D32 DQSB#5
FBC_QS_WP6 A32 DQSB#6
FBC_QS_WP7 B26 DQSB#7

FBC_WCK0 G14
FBC_WCK1 G15
FBC_WCK2 G11
FBC_WCK3 G12
FBC_WCK4 G27
FBC_WCK5 G28
FBC_WCK6 G24
FBC_WCK7 G25

FBC_CLK0 E17 CLKB0
FBC_CLK1 D17 CLKB#
FBC_CLK2 D23 CLKB1
FBC_CLK3 E23 CLKB1#

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CMDB3 <22>
CMDB4 <22,23>
CMDB5 <22,23>
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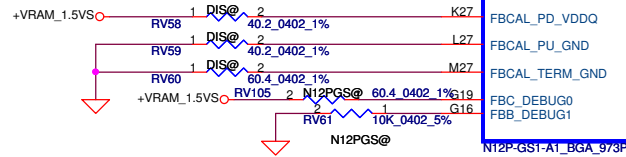
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GB2-128 Mode E - Mirror Mode Mapping

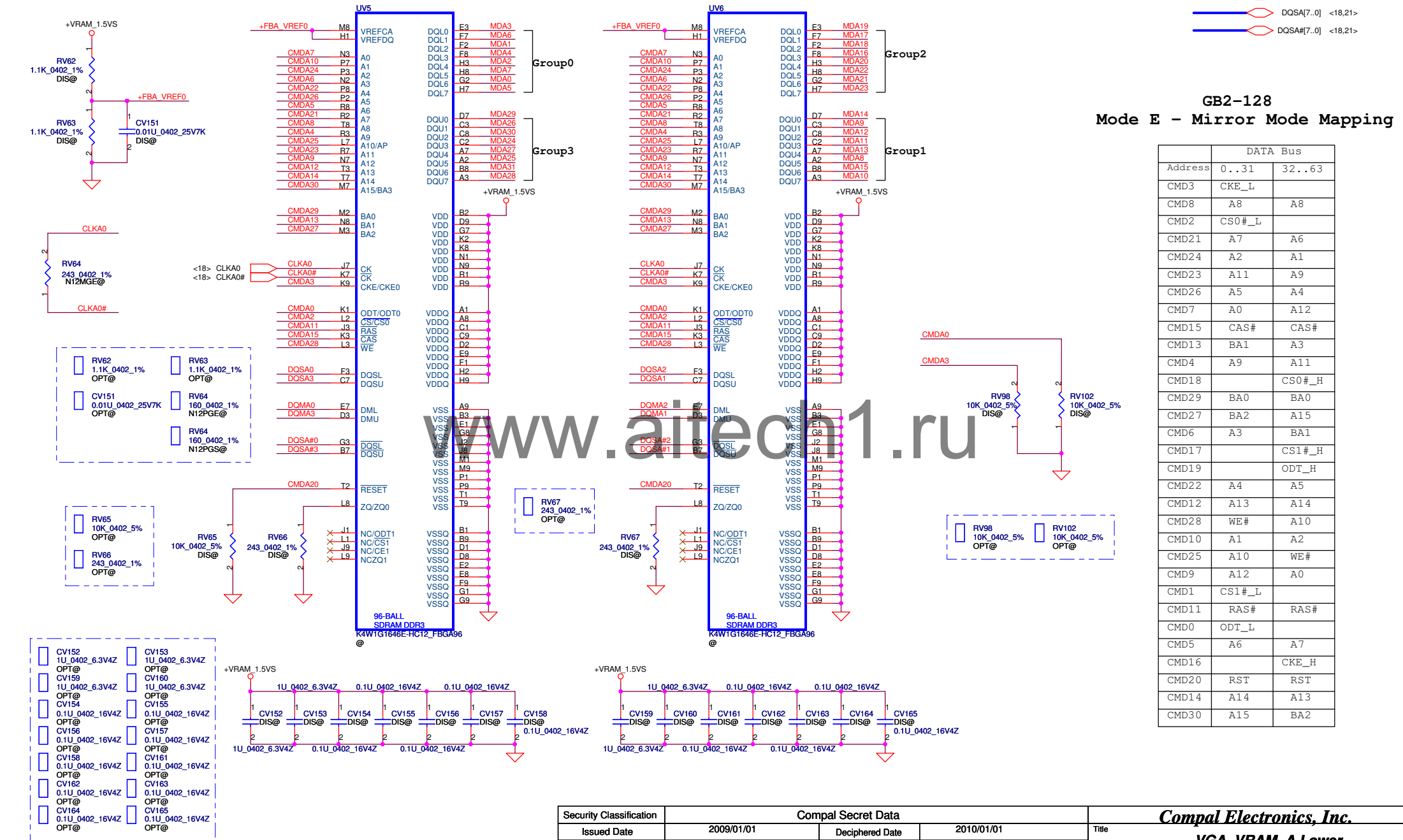
DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



Security Classification		Compal Secret Data	
Issued Date	2009/01/01	Deciphered Date	2010/01/01
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Compal Electronics, Inc.			Title
VGA_MEM Interface C			
Size	Document Number	Rev	0.1
Date:	Monday, August 02, 2010	Sheet	19 of 58

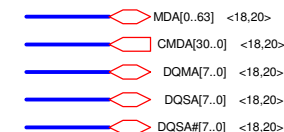
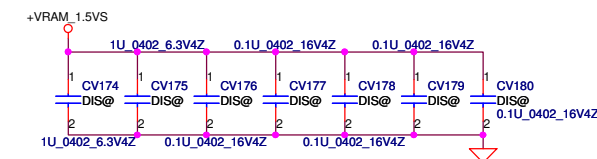
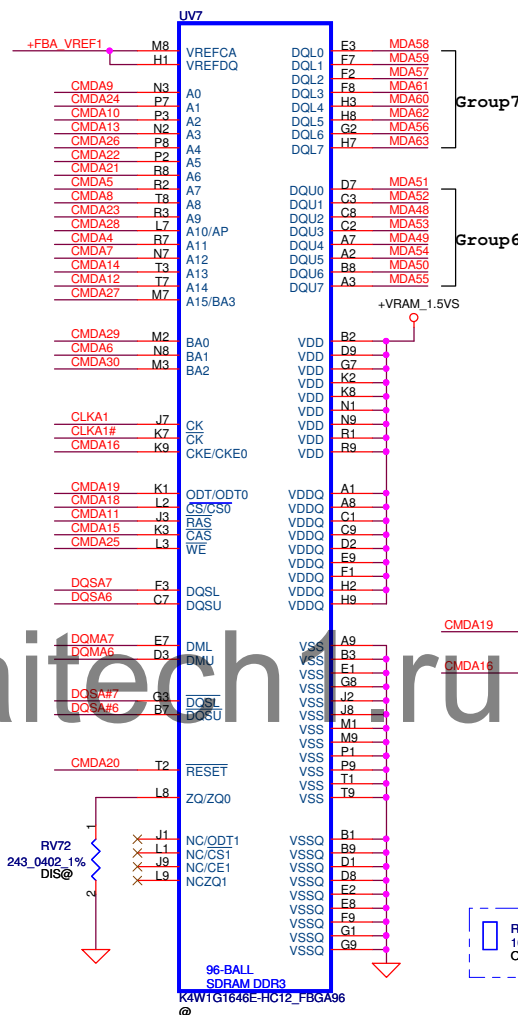
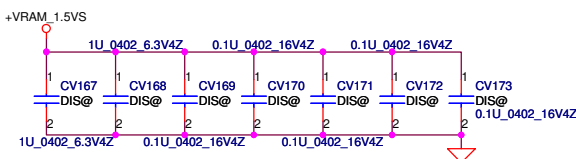
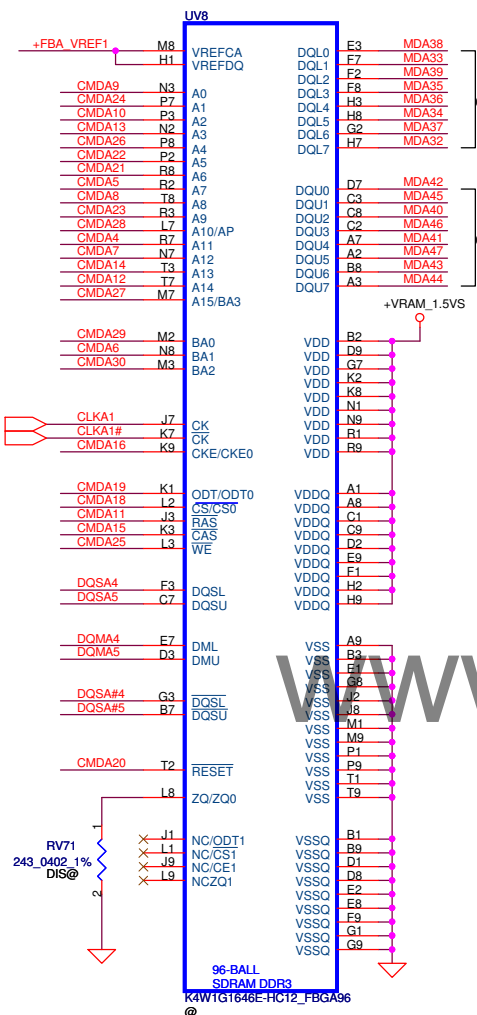
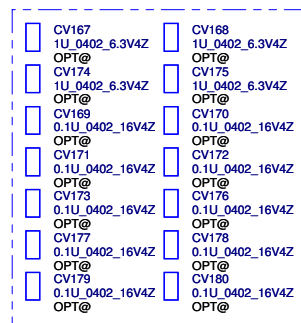
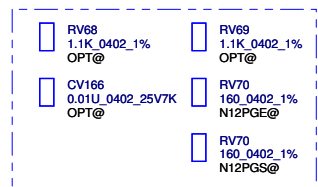
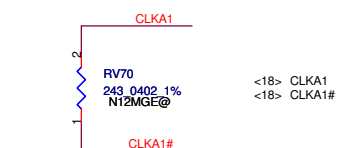
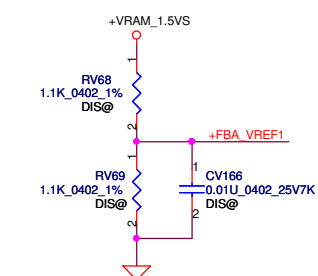
Memory Partition A - Lower 32 bits



GB2-128
Mode E - Mirror Mode Mapping

Address	DATA Bus
CMD3	CKE_L
CMD8	A8
CMD2	CS0#_L
CMD21	A7
CMD24	A2
CMD23	A11
CMD26	A5
CMD7	A0
CMD15	CAS#
CMD13	BA1
CMD4	A9
CMD18	CS0#_H
CMD29	BA0
CMD27	BA2
CMD6	A3
CMD17	CS1#_H
CMD19	ODT_H
CMD22	A4
CMD12	A13
CMD28	WE#
CMD10	A1
CMD25	A10
CMD9	A12
CMD1	CS1#_L
CMD11	RAS#
CMD0	ODT_L
CMD5	A6
CMD16	CKE_H
CMD20	RST
CMD14	A14
CMD30	A15

Memory Partition A - Upper 32 bits

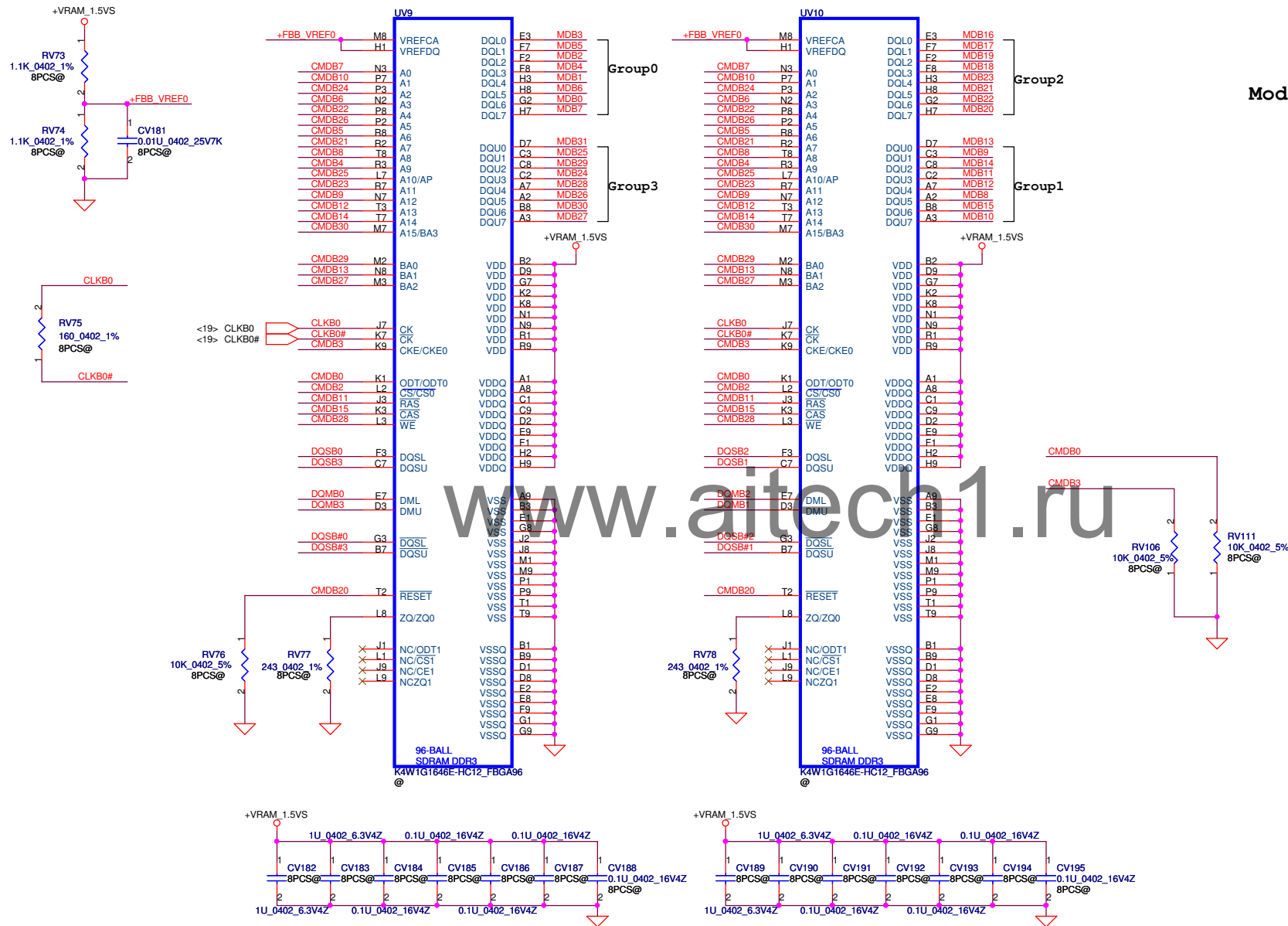


GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification		Compal Secret Data		Compal Electronics, Inc. VGA_VRAM_A Upper	
Issued Date	2009/01/01	Deciphered Date	2010/01/01		
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				Size	Document Number PHQAA LA-6831P M/B
				Date:	Monday, August 02, 2010 Sheet 21 of 58

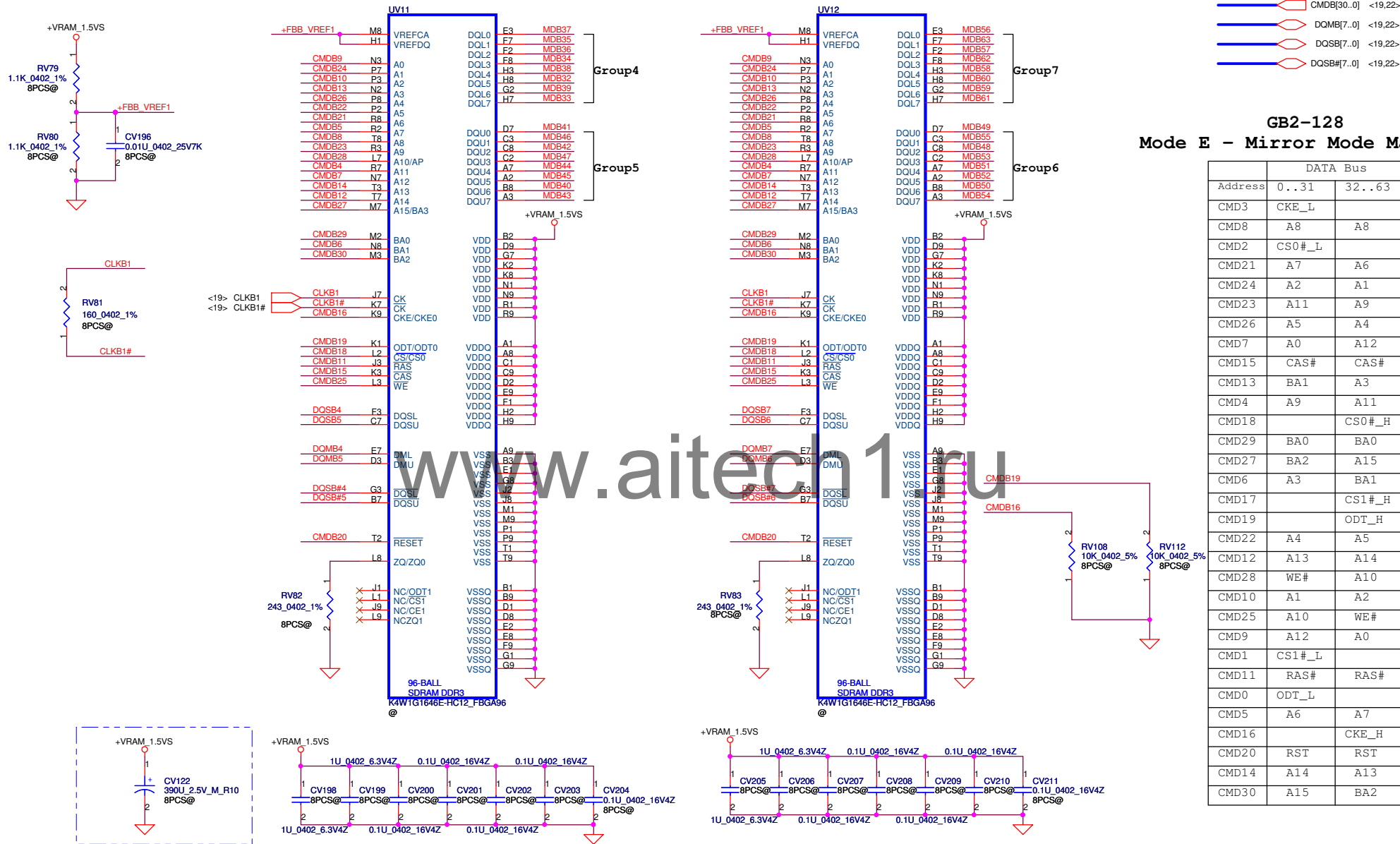
Memory Partition C - Lower 32 bits

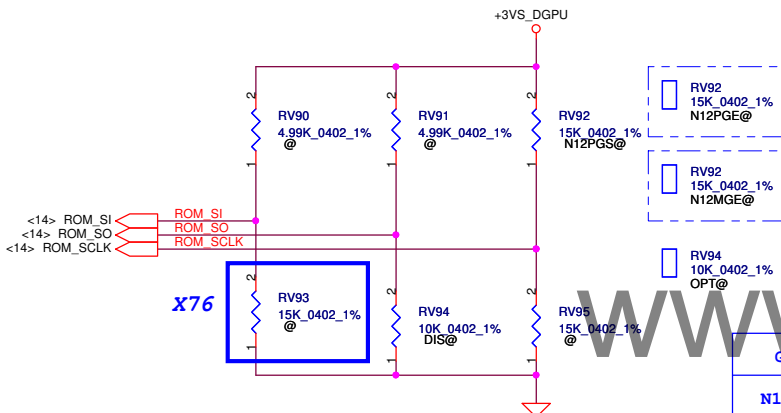
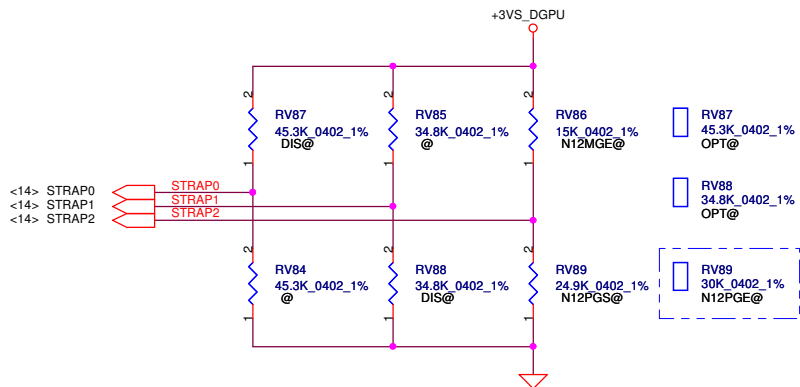


GB2-128
Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Memory Partition C - Upper 32 bits





GPU	DeviceID	ROM_SCLK	STRAP2
N12M-GE	0x0A7A	Pull up 15K	Pull up 15K
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GE	0x0DF5	Pull up 15K	Pull down 30K

Hynix H5TQ1G63BFR-12C SA000032400	512M	0010	PD 15K
	1G	0010	PD 15K
Samsung K4W1G1646E-HC12 SA000035700	512M	0011	PD 20K
	1G	0011	PD 20K

SD034150280

SD034200280

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User [3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

Security Classification	Compal Secret Data				Compal Electronics, Inc.		
Issued Date	2009/01/01	Deciphered Date	2010/01/01		VGA_MSIC		
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					Date:	Monday, August 02, 2010	Sheet 24 of 58

OPTIMUS

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 <31> LCD_TXOUT1+ 1 OPT@ 2 LVDS_TXOUT1+
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 R500 0.0402_5% UMA@

Close to LVDS Connector

DISCRETE

<14> VGA_TXOUT0+ 1 DIS@ 2 LVDS_TXOUT0+
 <14> VGA_TXOUT0- 1 DIS@ 2 LVDS_TXOUT0-
 <14> VGA_TXOUT1+ 1 DIS@ 2 LVDS_TXOUT1+
 <14> VGA_TXOUT1- 1 DIS@ 2 LVDS_TXOUT1-
 <14> VGA_TXOUT2+ 1 DIS@ 2 LVDS_TXOUT2+
 <14> VGA_TXOUT2- 1 DIS@ 2 LVDS_TXOUT2-
 <14> VGA_TXCLK+ 1 DIS@ 2 LVDS_TXCLK+
 <14> VGA_TXCLK- 1 DIS@ 2 LVDS_TXCLK-
 <13> VGA_EDID_CLK 1 DIS@ 2 LVDS_EDID_CLK
 <13> VGA_EDID_DATA 1 DIS@ 2 LVDS_EDID_DATA
 <13> VGA_BL_PWM 1 DIS@ 2 LED_PWM
 <13> VGA_ENVDD 1 DIS@ 2 LCD_ENVDD
 <13> VGA_ENBKL 1 DIS@ 2 EC_ENBKL

Close to LVDS Connector

DISCRETE for Full-HD and 3D LVDS Panel

<14> VGA_TZOUT0+ 1 3D@ 2 LVDS_TZOUT0+
 <14> VGA_TZOUT0- 1 3D@ 2 LVDS_TZOUT0-
 <14> VGA_TZOUT1+ 1 3D@ 2 LVDS_TZOUT1+
 <14> VGA_TZOUT1- 1 3D@ 2 LVDS_TZOUT1-
 <14> VGA_TZOUT2+ 1 3D@ 2 LVDS_TZOUT2+
 <14> VGA_TZOUT2- 1 3D@ 2 LVDS_TZOUT2-
 <14> VGA_TZCLK+ 1 3D@ 2 LVDS_TZCLK+
 <14> VGA_TZCLK- 1 3D@ 2 LVDS_TZCLK-

Close to LVDS1 Connector

DISCRETE for Full-HD and 3D eDP Panel

<14> VGA_EDP_TX0+ 1 C880 20.1U_0402_16V7K LVDS_TZOUT0+
 <14> VGA_EDP_TX0- 1 C881 20.1U_0402_16V7K LVDS_TZOUT0-
 <14> VGA_EDP_TX1+ 1 C882 20.1U_0402_16V7K LVDS_TZOUT1+
 <14> VGA_EDP_TX1- 1 C883 20.1U_0402_16V7K LVDS_TZOUT1-
 <14> VGA_EDP_TX2+ 1 C884 20.1U_0402_16V7K LVDS_TZOUT2+
 <14> VGA_EDP_TX2- 1 C885 20.1U_0402_16V7K LVDS_TZOUT2-
 <14> VGA_EDP_TX3+ 1 C886 20.1U_0402_16V7K LVDS_TZCLK+
 <14> VGA_EDP_TX3- 1 C887 20.1U_0402_16V7K LVDS_TZCLK-

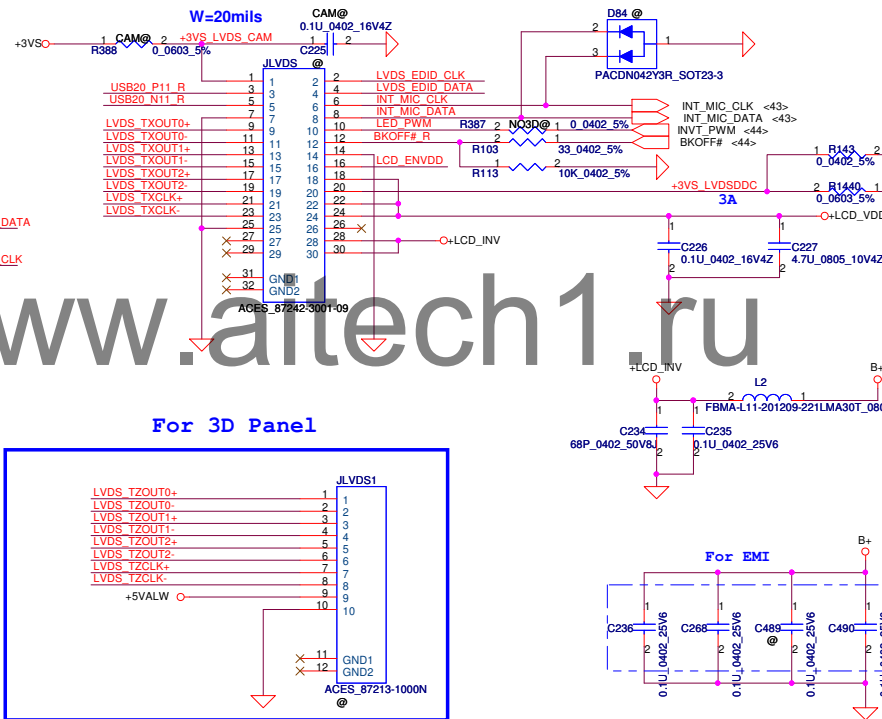
Close to LVDS1 Connector

<14> VGA_EDP_AUX 1 C888 20.1U_0402_16V7K LVDS_EDID_CLK
 <14> VGA_EDP_AUX 1 C889 20.1U_0402_16V7K LVDS_EDID_DATA

Close to LVDS Connector

Reserve for EMI request

LCD/PANEL BD. Conn.



For 3D Panel

For EMI

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OPTIMUS

<31> UMA_CRT_R	1 OPT@ 2	CRT_R
<31> UMA_CRT_G	1 OPT@ 2	CRT_G
<31> UMA_CRT_B	1 OPT@ 2	CRT_B
<31> UMA_CRT_HSYNC	1 OPT@ 2	CRT_HSYNC
<31> UMA_CRT_VSYNC	1 OPT@ 2	CRT_VSYNC
<31> UMA_CRT_CLK	1 OPT@ 2	CRT_CLK
<31> UMA_CRT_DATA	1 OPT@ 2	CRT_DATA

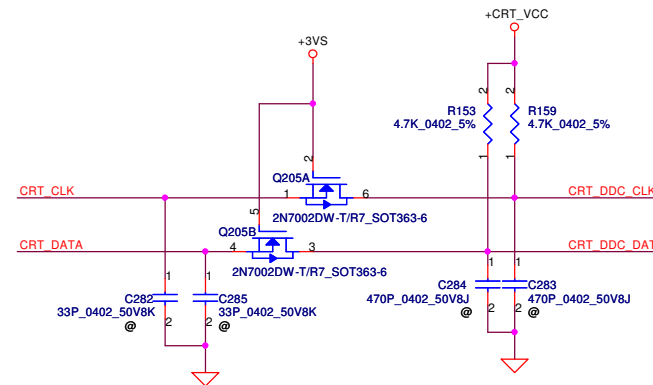
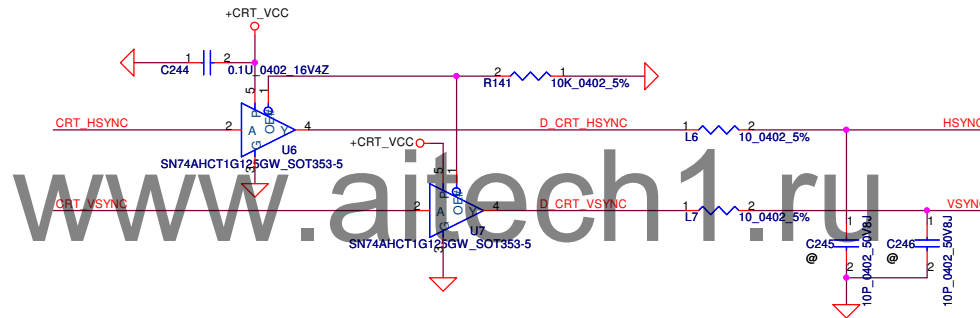
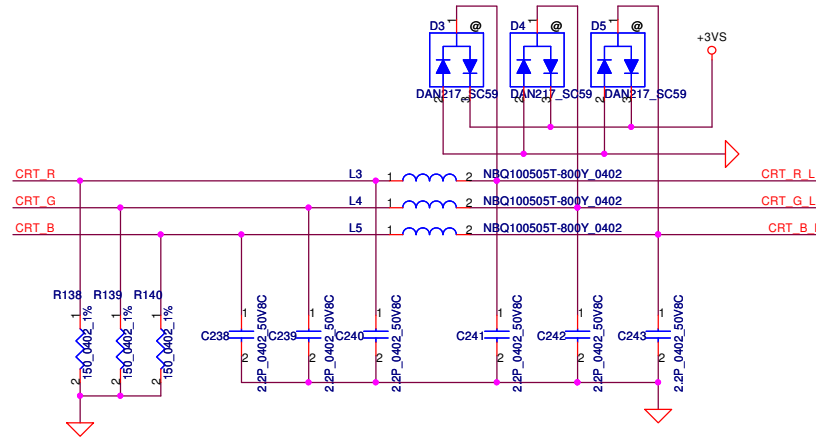
Close to CRT Connector

R200 0.0402_5% UMA@	R204 0.0402_5% UMA@	R211 0.0402_5% UMA@
R213 0.0402_5% UMA@	R235 0.0402_5% UMA@	R236 0.0402_5% UMA@
R261 0.0402_5% UMA@		

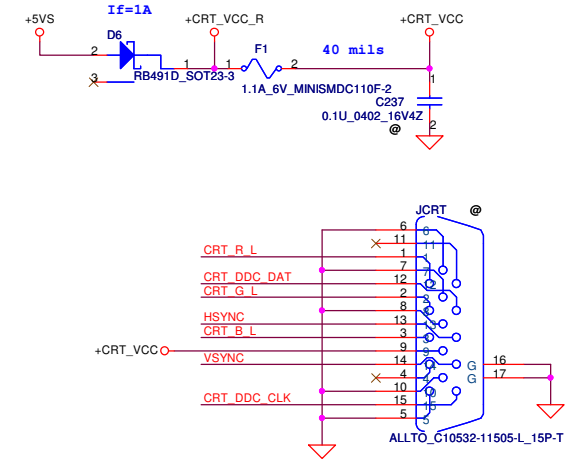
DISCRETE

<13> VGA_CRT_R	1 DIS@ 2	CRT_R
<13> VGA_CRT_G	1 DIS@ 2	CRT_G
<13> VGA_CRT_B	1 DIS@ 2	CRT_B
<13> VGA_CRT_HSYNC	1 DIS@ 2	CRT_HSYNC
<13> VGA_CRT_VSYNC	1 DIS@ 2	CRT_VSYNC
<13> VGA_CRT_CLK	1 DIS@ 2	CRT_CLK
<13> VGA_CRT_DATA	1 DIS@ 2	CRT_DATA

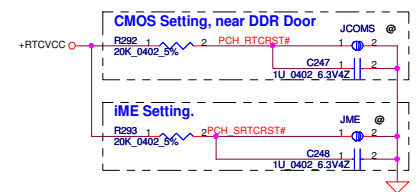
Close to CRT Connector



CRT CONNECTOR

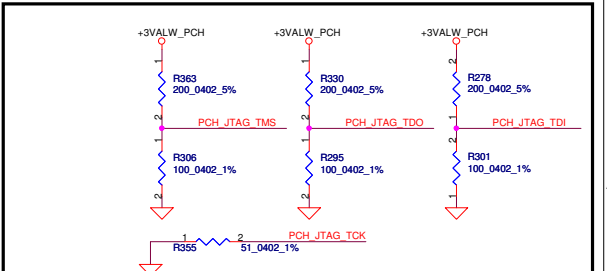
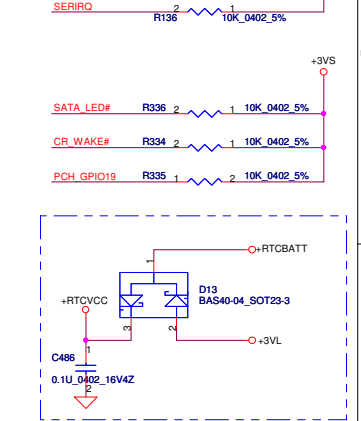
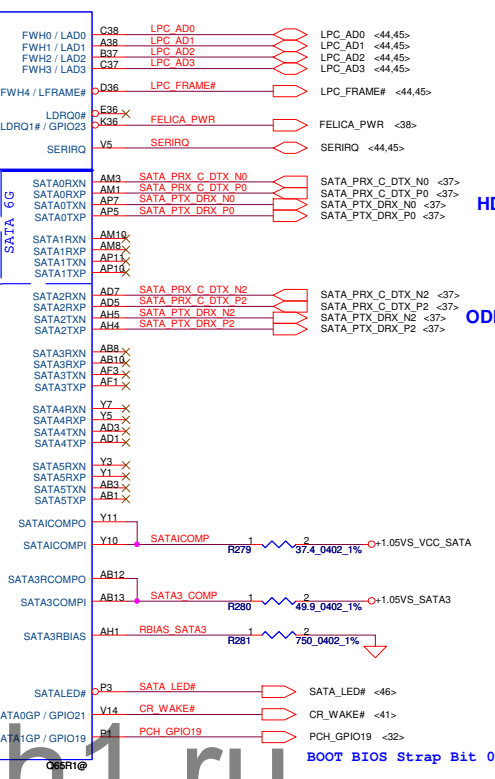
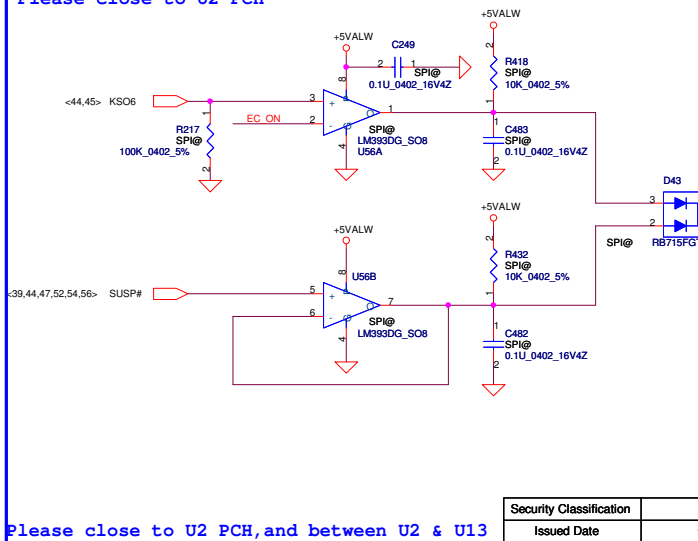
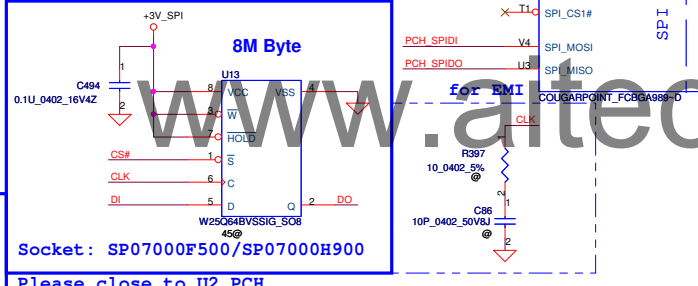
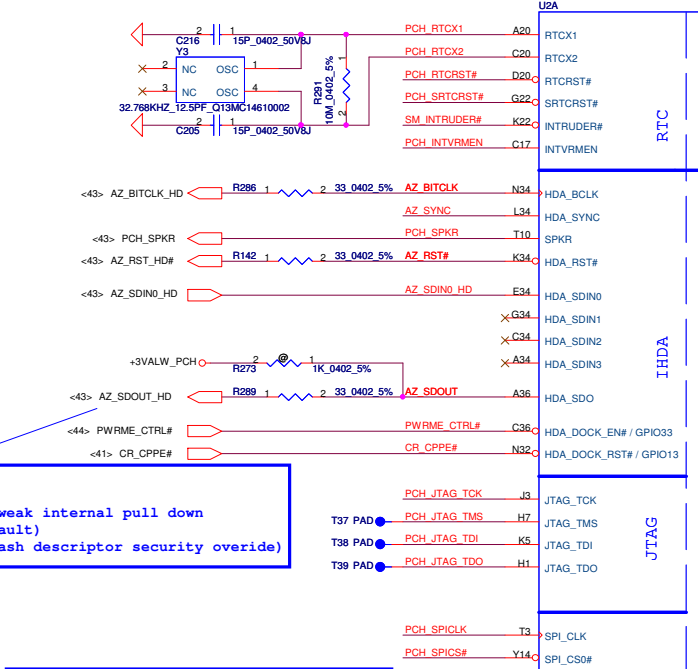
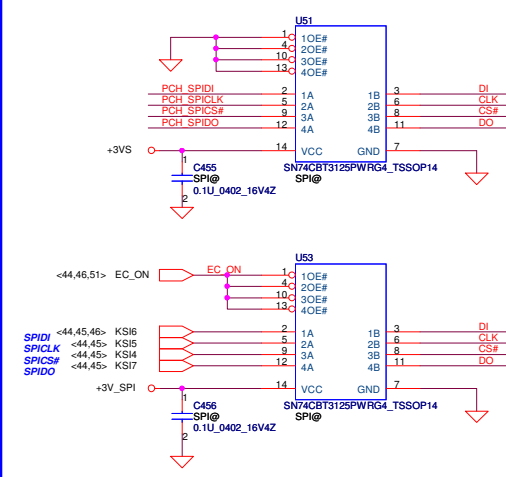
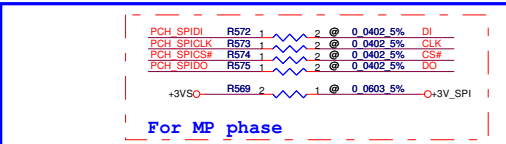
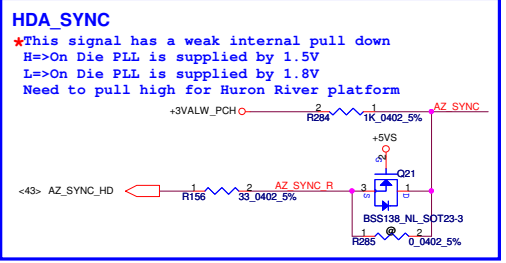
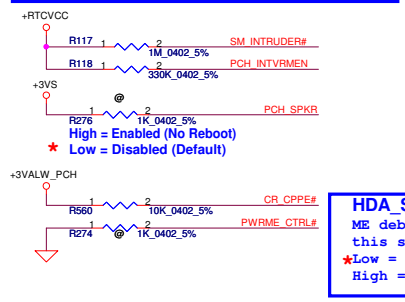


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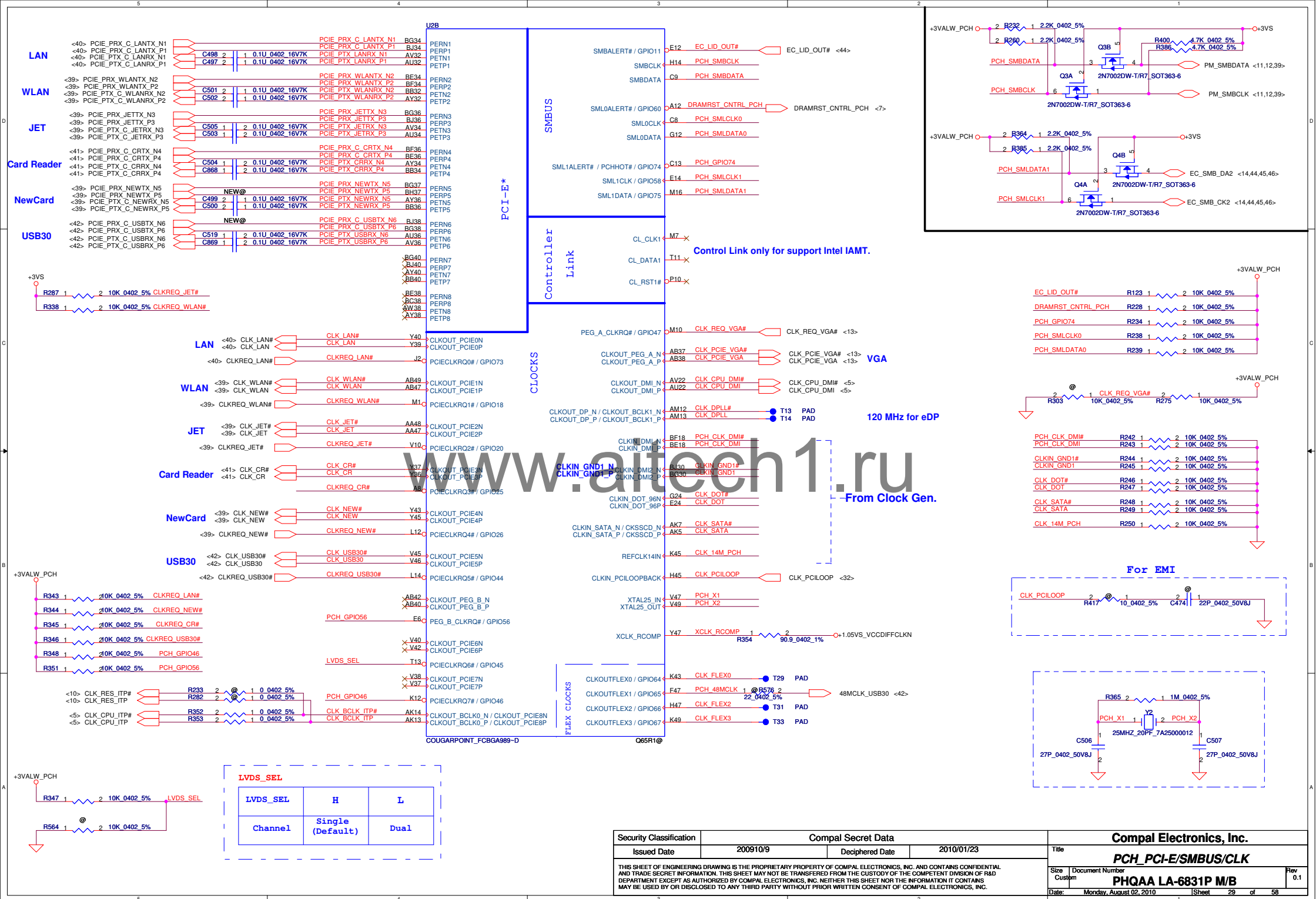


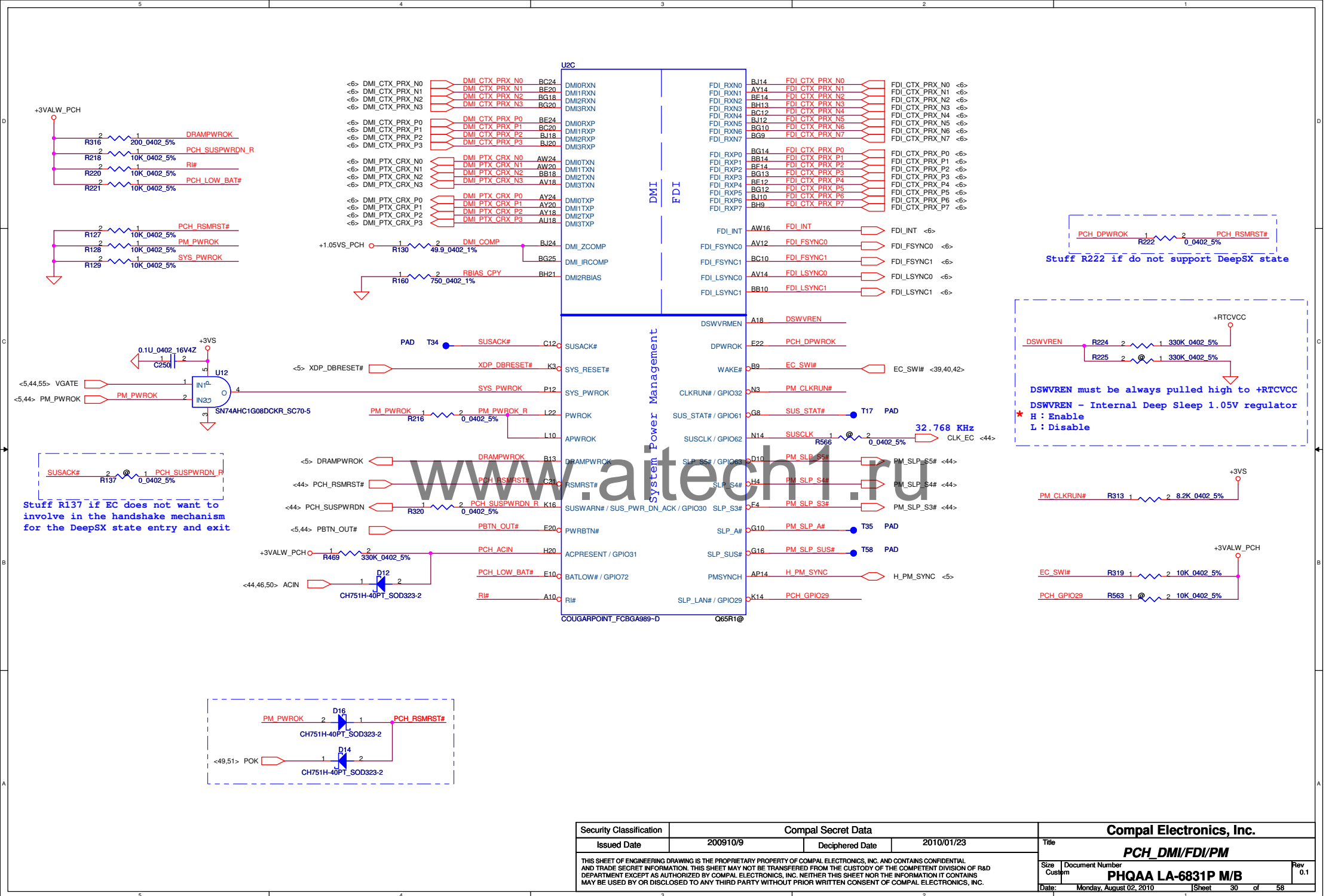
Integrated SUS 1.05V VRM Enable

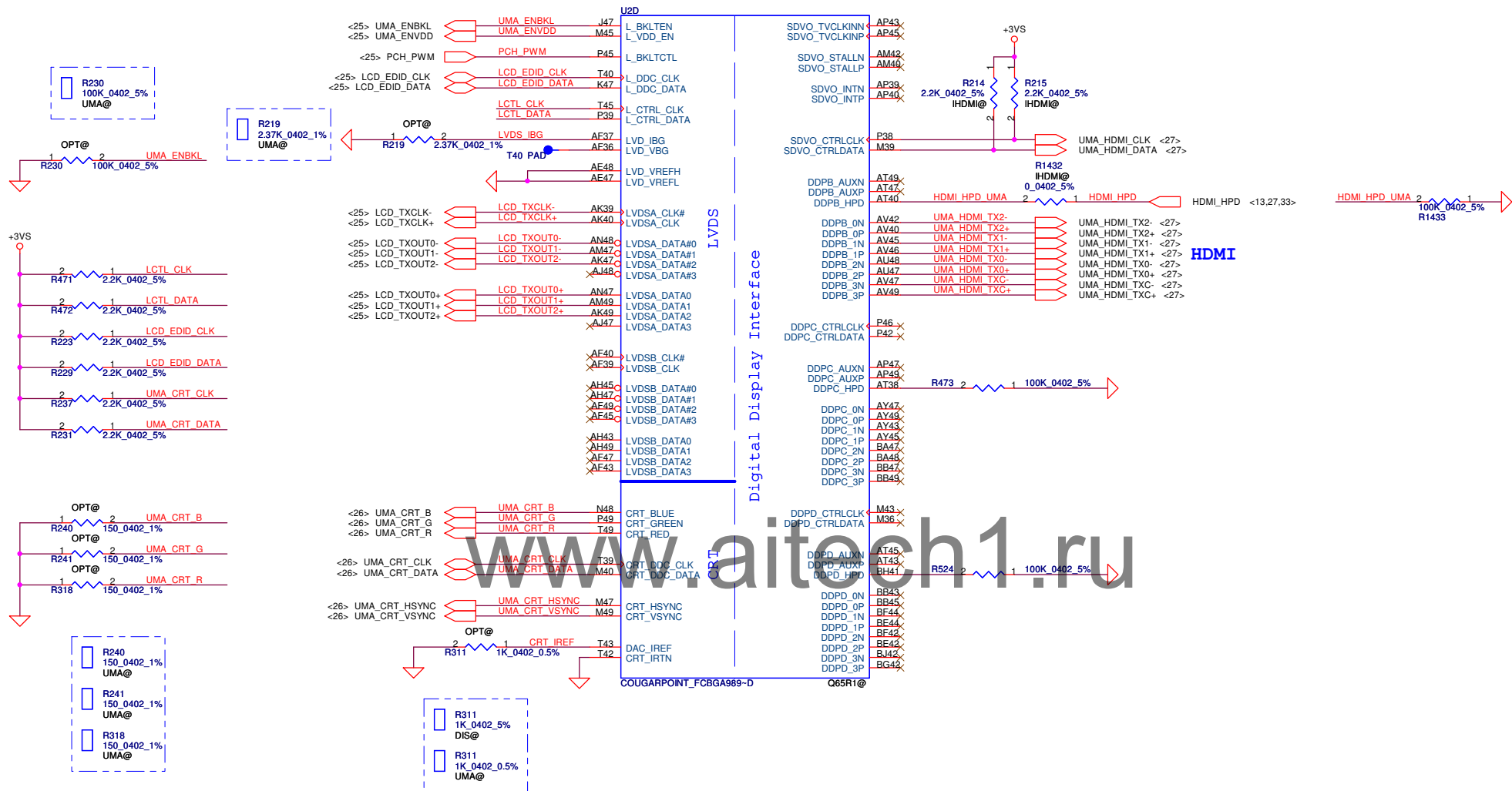
PCH_INTVRMEN High - Enable Internal VRs (must be always pulled high)



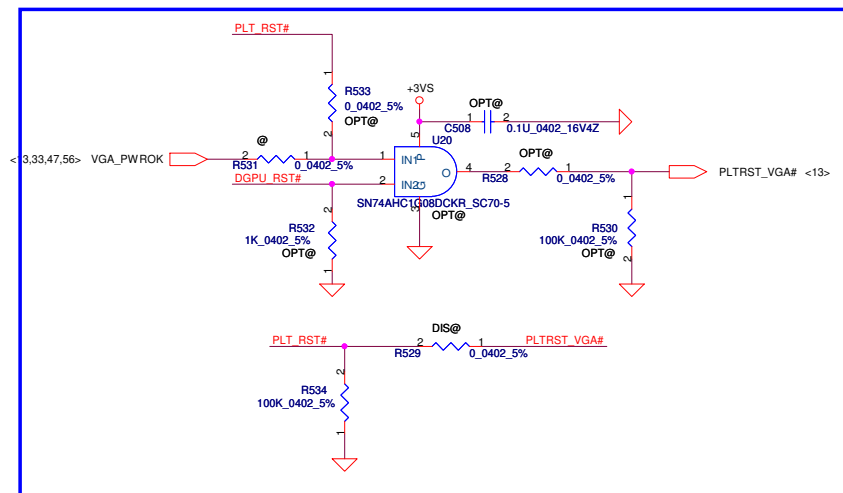
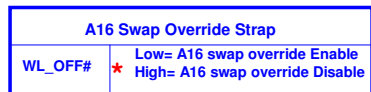
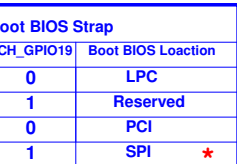
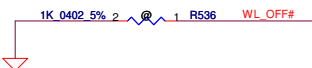
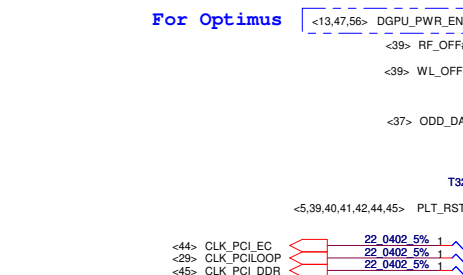
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	PCH_HDA/JTAG/SATA/SPI/LPC	
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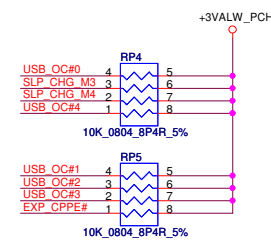
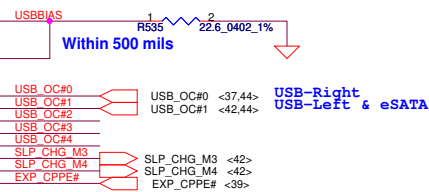
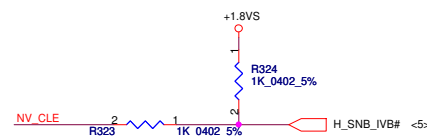
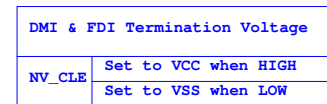
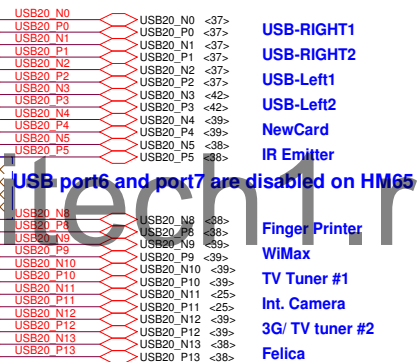




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Size	Custom	Document Number	PHQAA LA-6831P M/B	Rev	0.1
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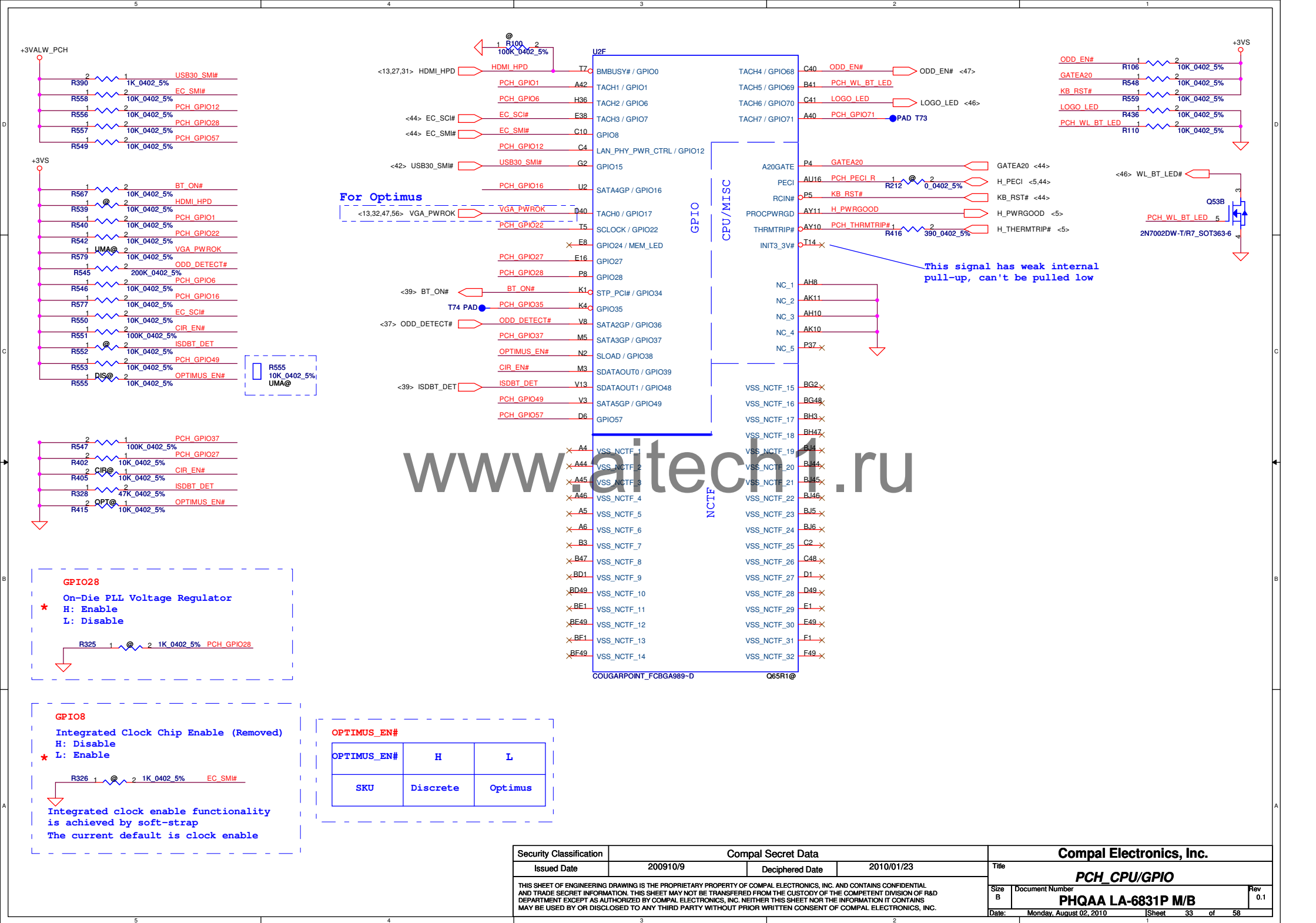
For Optimus

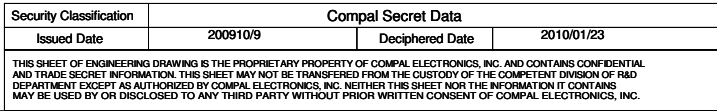


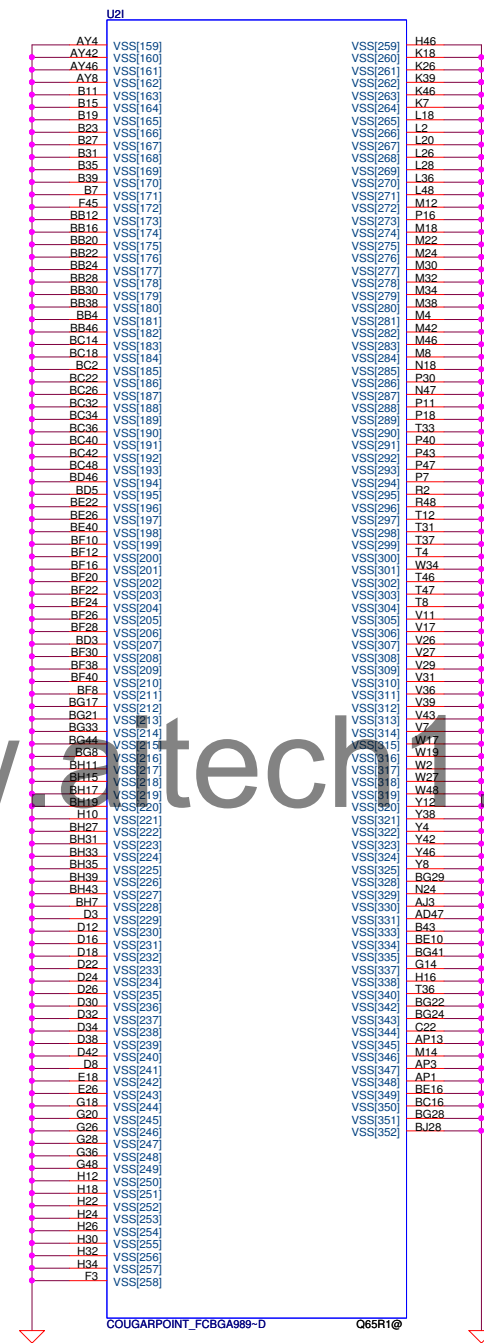
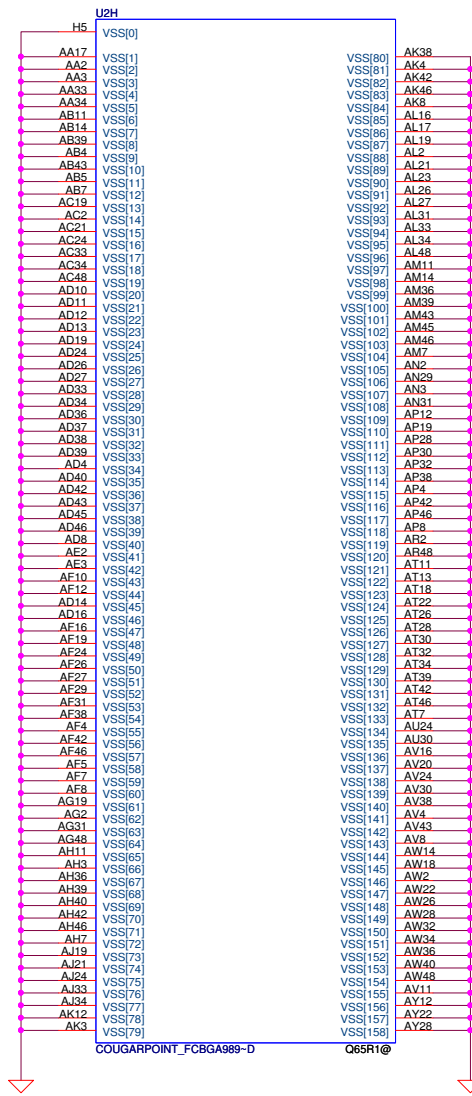
Boot BIOS Strap		
RF_OFF#	PCH_GPIO19	Boot BIOS Loaction
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI ★

A16 Swap Override Strap	
WL_OFF#	★ Low= A16 swap override Enable High= A16 swap override Disable

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				Size	Document Number	Rev	
				Cust	PHQAA LA-6831P M/B	0.1	
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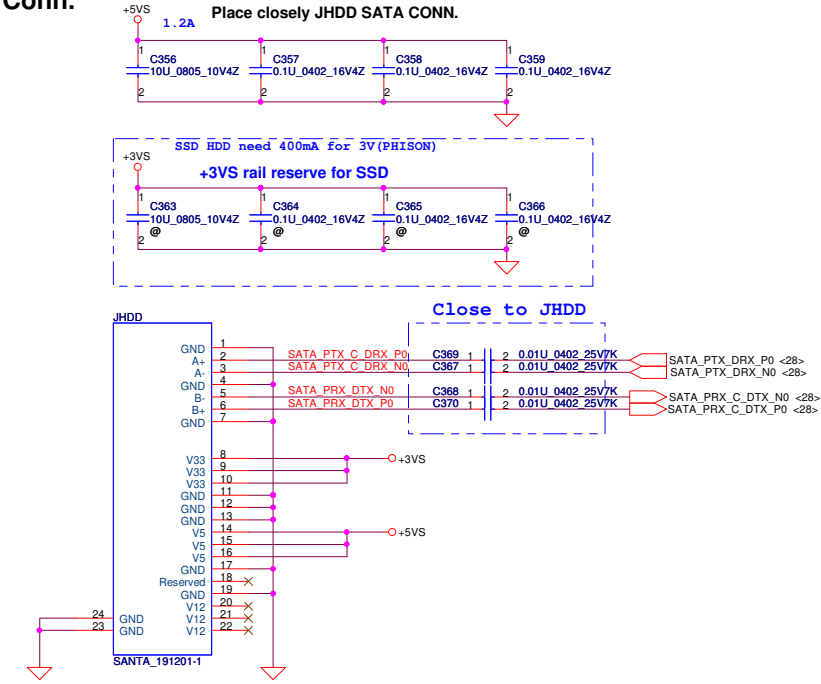




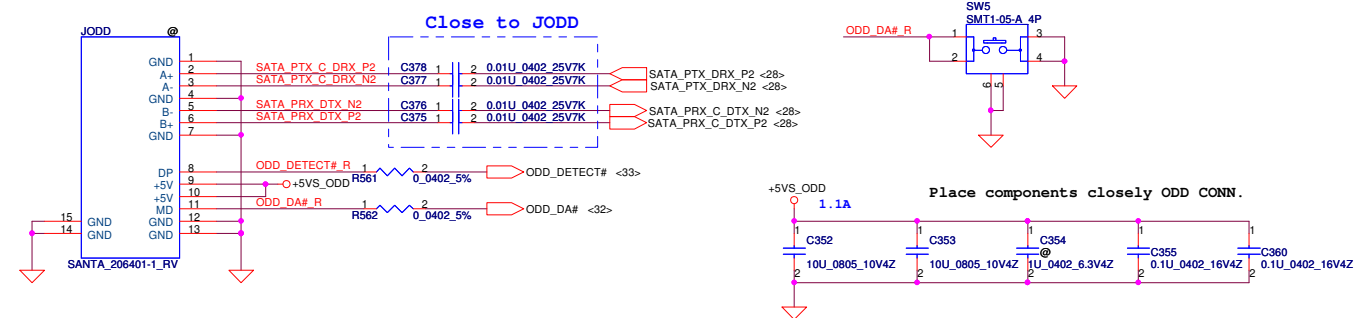


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				Size	Document Number	Rev
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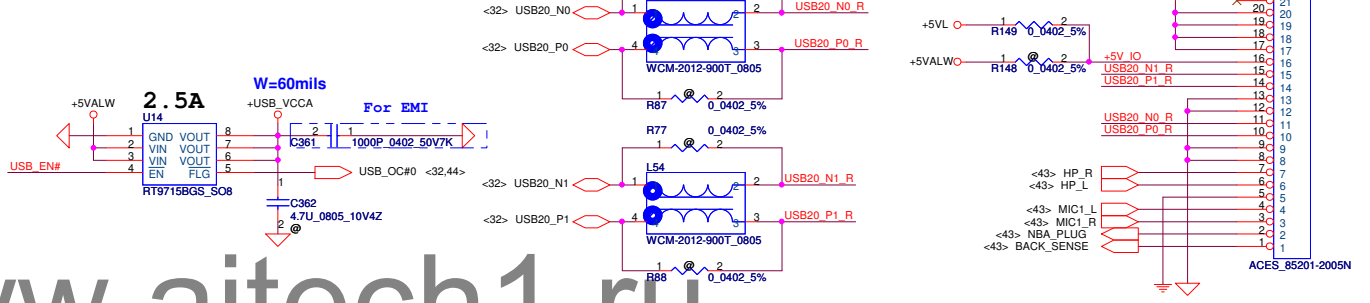
SATA HDD Conn.



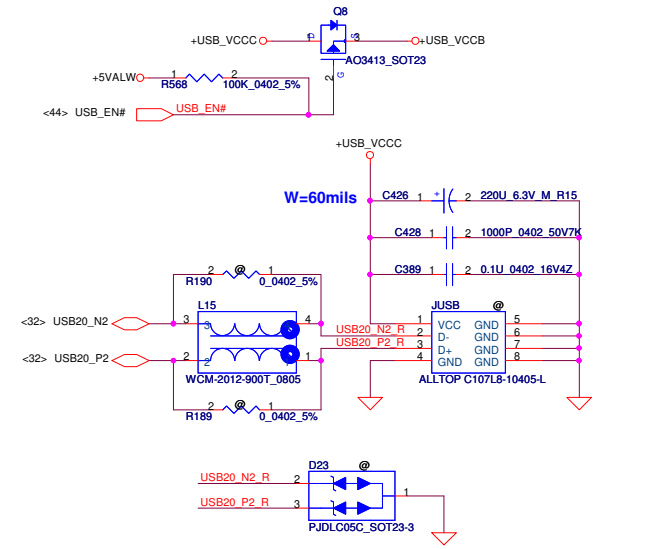
SATA ODD Conn



USB Board@ Right Side

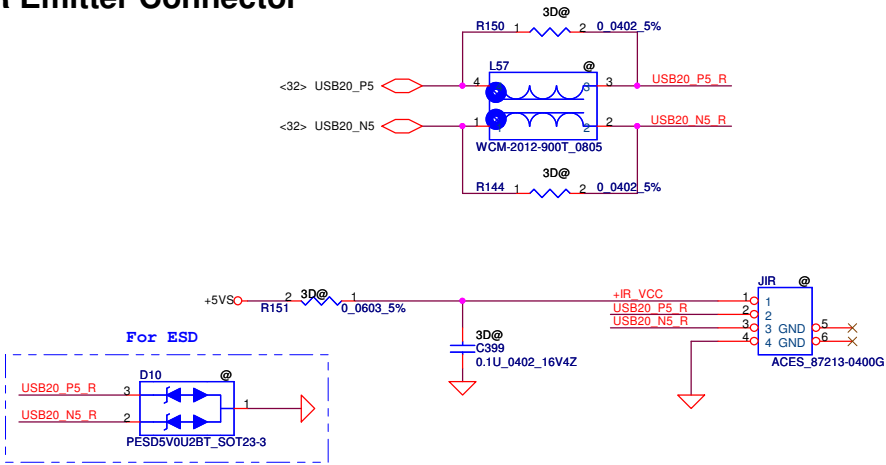


USB Board@ Left Side

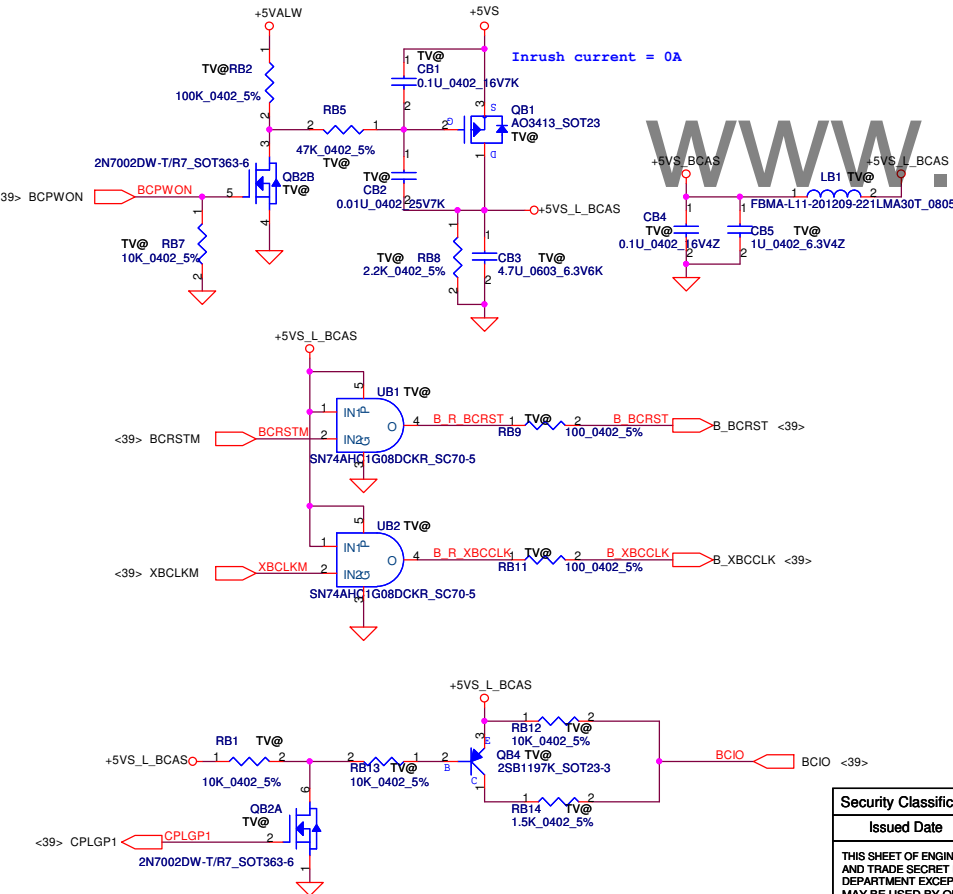


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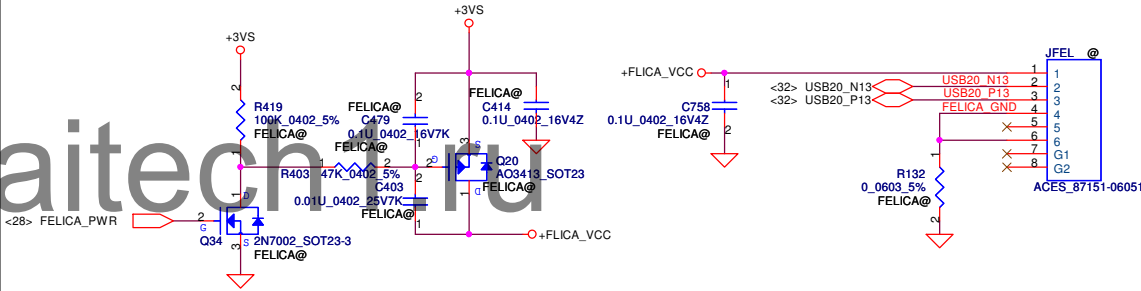
IR Emitter Connector



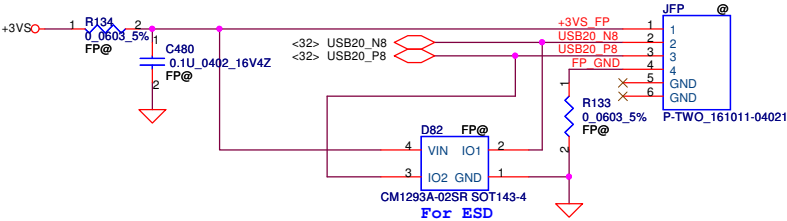
B-CAS Circuit



Felica

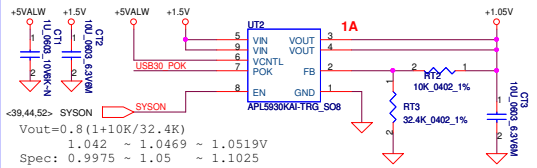


Finger printer

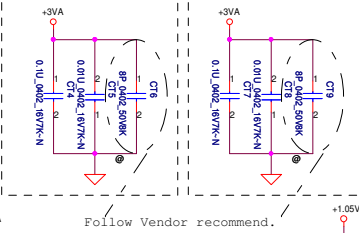


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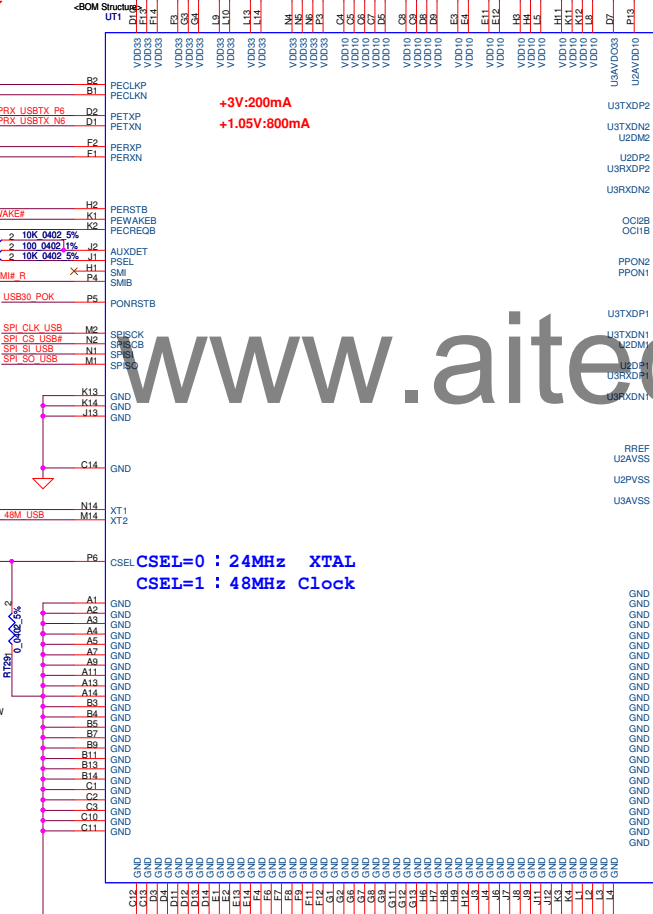
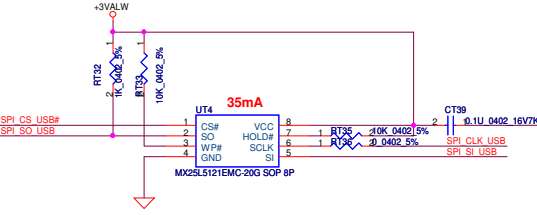
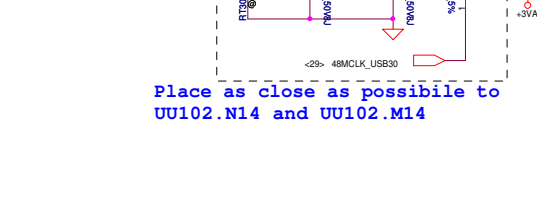
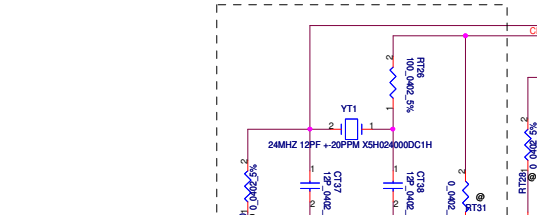
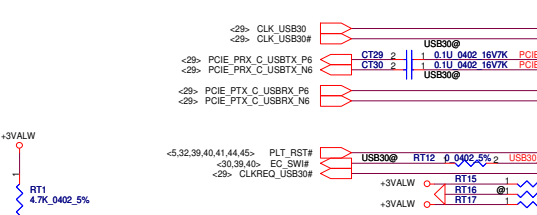
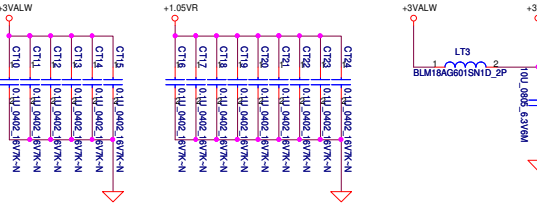
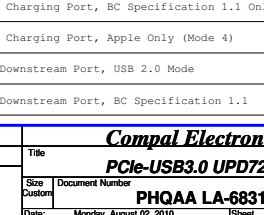
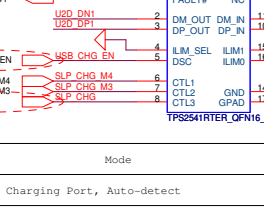
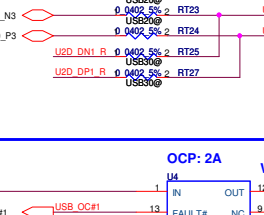
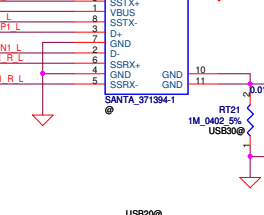
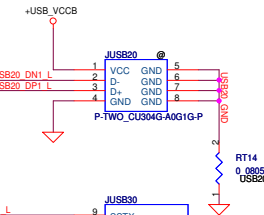
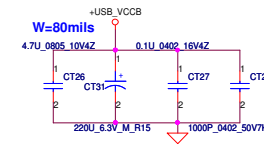
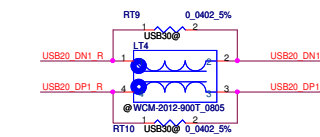
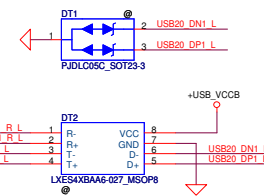
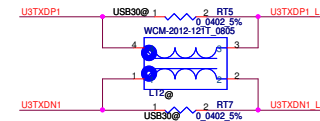
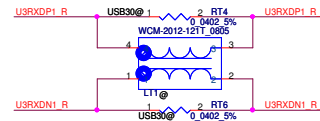
+1.5V to +1.05V Transfer



Close to U102.D7 Close to U102.P13



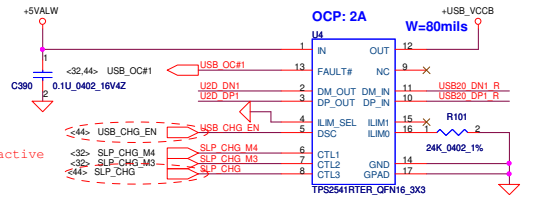
Follow Vendor recommend.



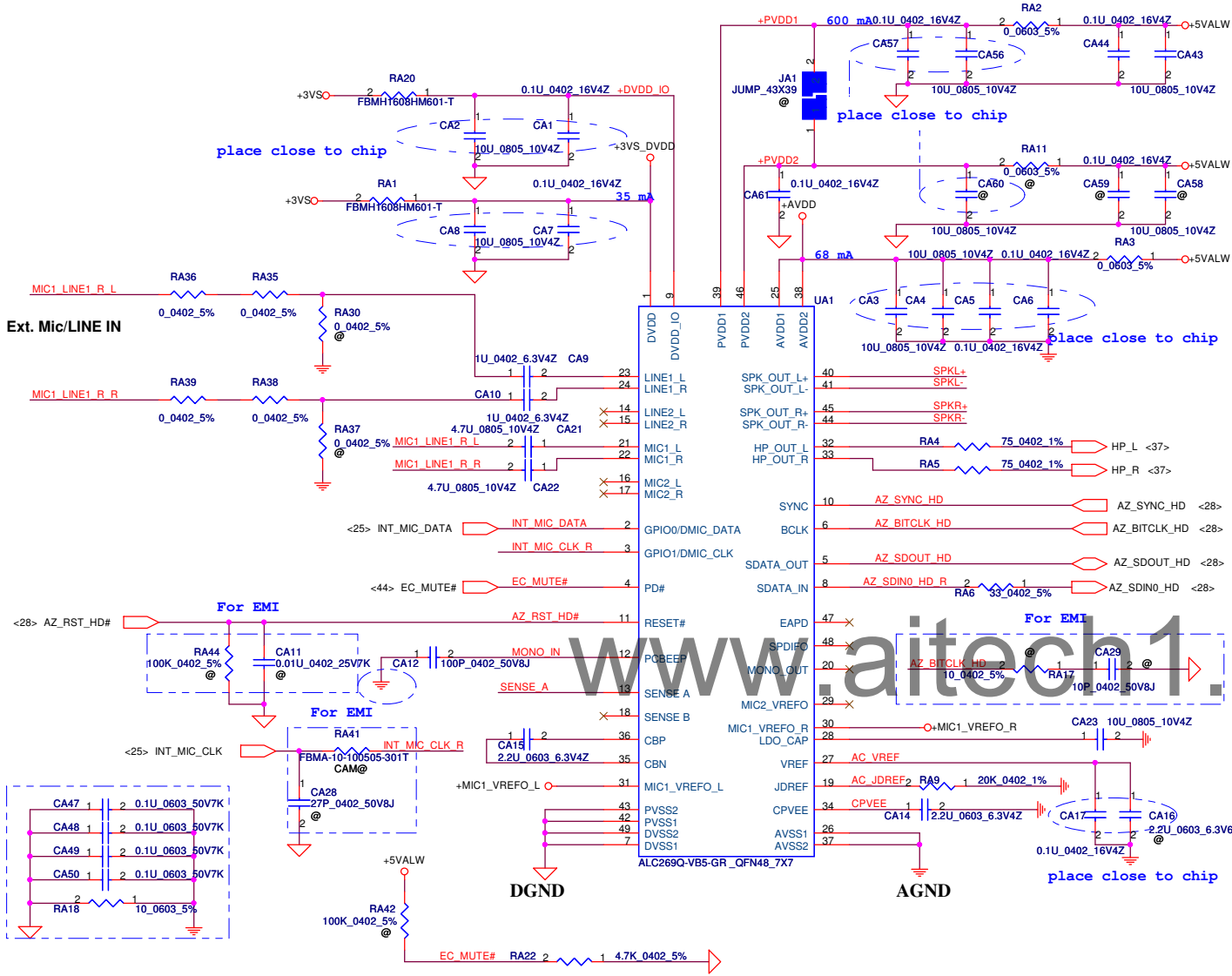
www.aitecn1.ru

USB Sleep & Charge Auto-Mode

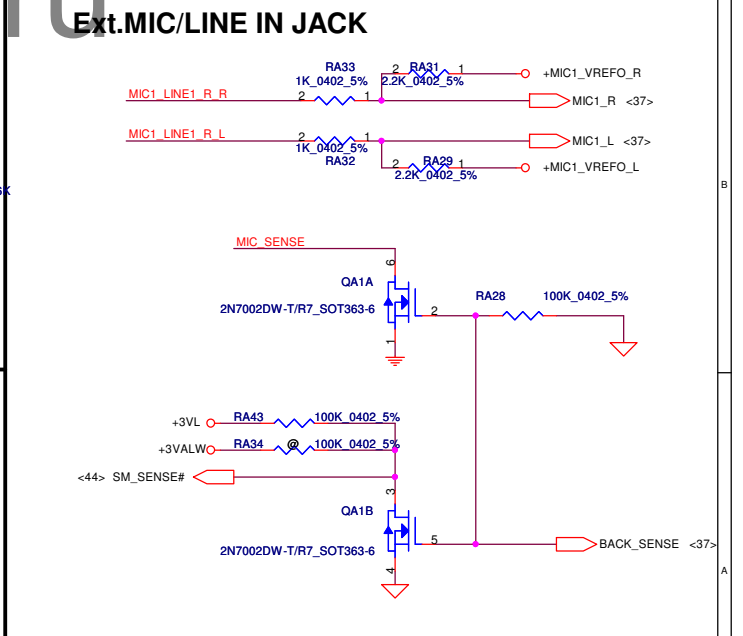
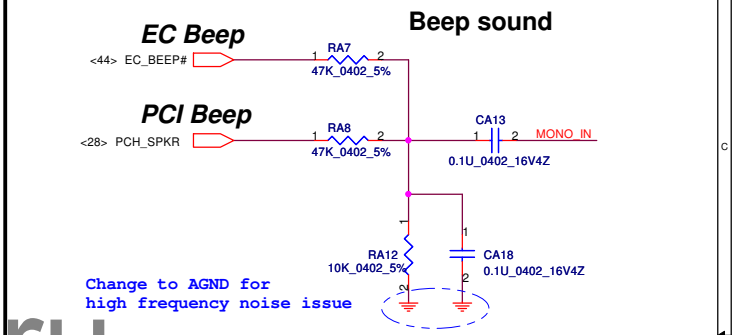
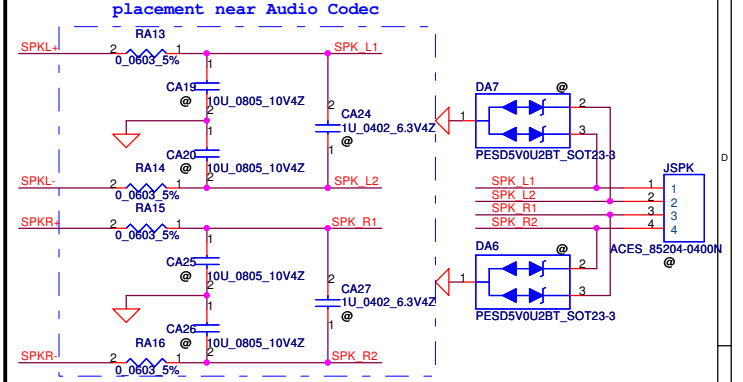
07/08/2010
Need EC to set these signals to high active
SLP_CHG, USB_CHG_EN



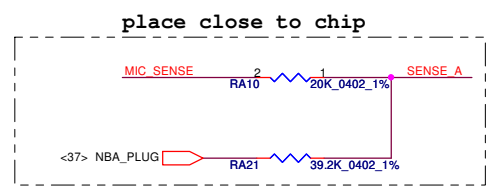
SLP_CHG_M4	SLP_CHG_M3	SLP_CHG	Mode
0	0	X(1)	Dedicated Charging Port, Auto-detect
0	1	X(1)	Dedicated Charging Port, BC Specification 1.1 Only (Mode 3)
1	0	X(1)	Dedicated Charging Port, Apple Only (Mode 4)
1	1	0	Standard Downstream Port, USB 2.0 Mode
1	1	1	Charging Downstream Port, BC Specification 1.1

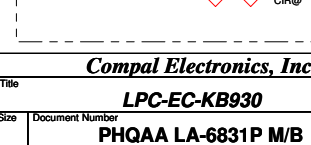
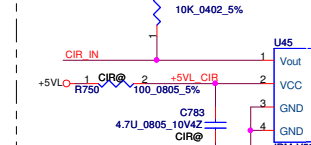
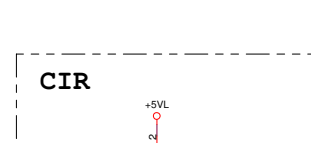
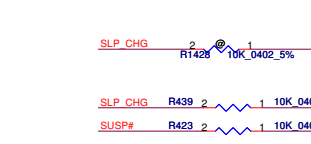
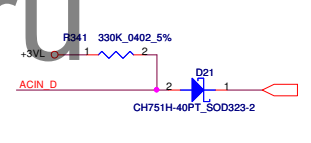
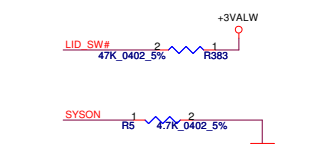
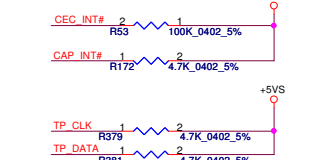
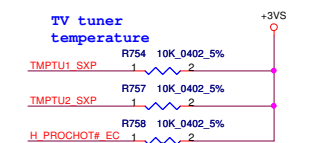
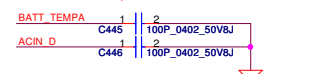
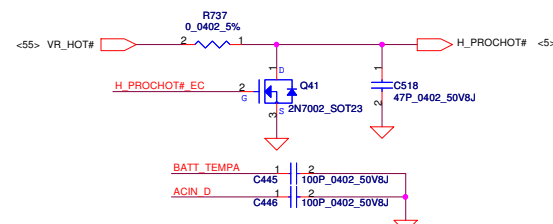
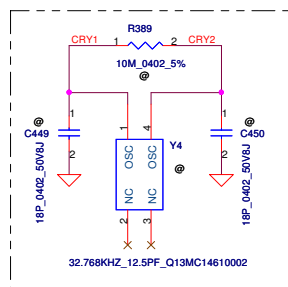
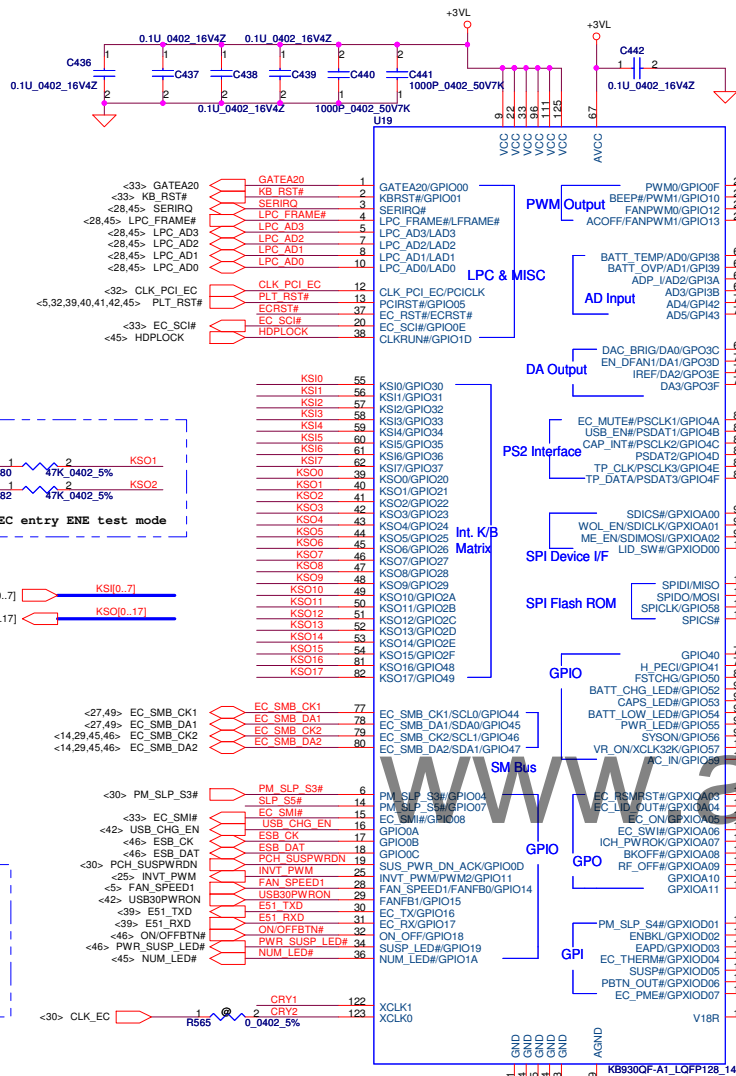
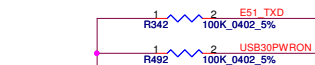
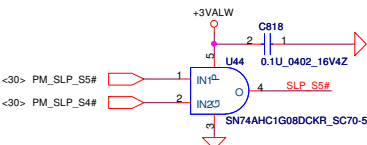
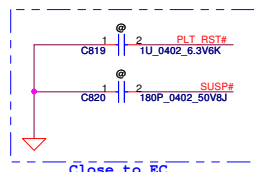
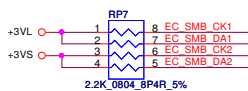
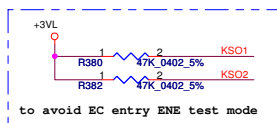
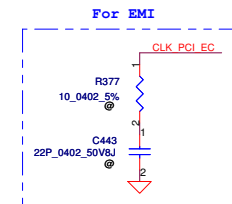


Speaker Connector



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

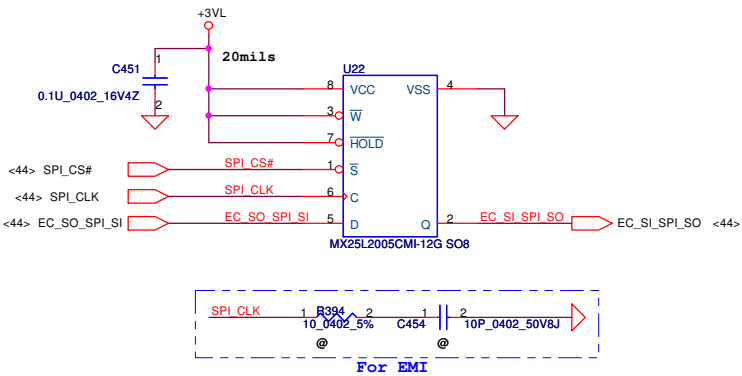




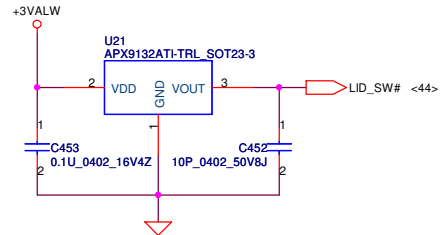
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Issued Date	200910/9	Deciphered Date	2010/01/23	Title	LPC-EC-KB930
Size		Document Number		Rev	0.1
Date:		Monday, August 02, 2010		Sheet	44 of 58

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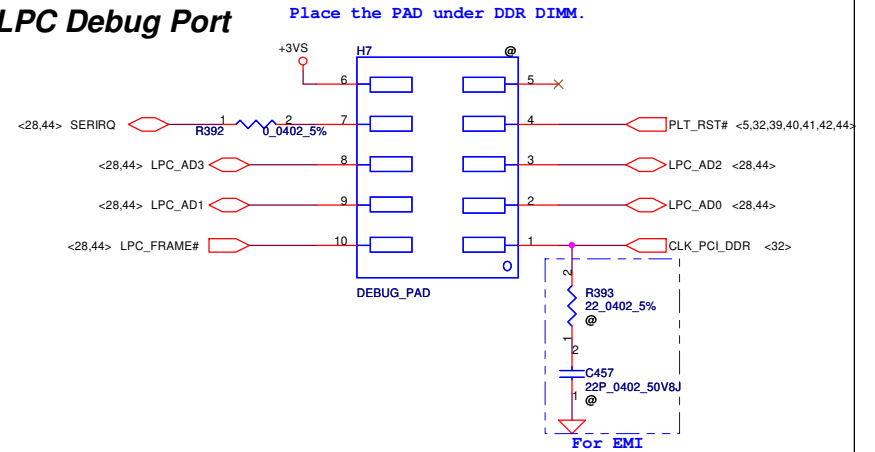
SPI Flash (256KB)



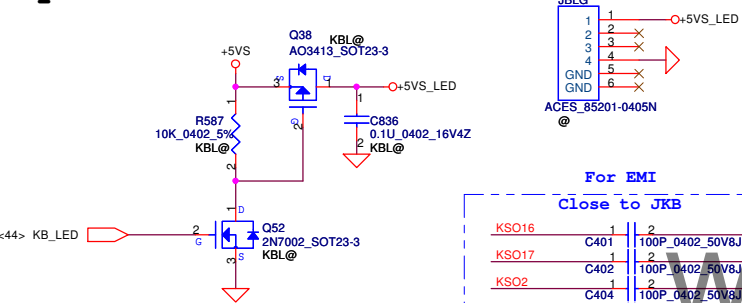
Lid SW



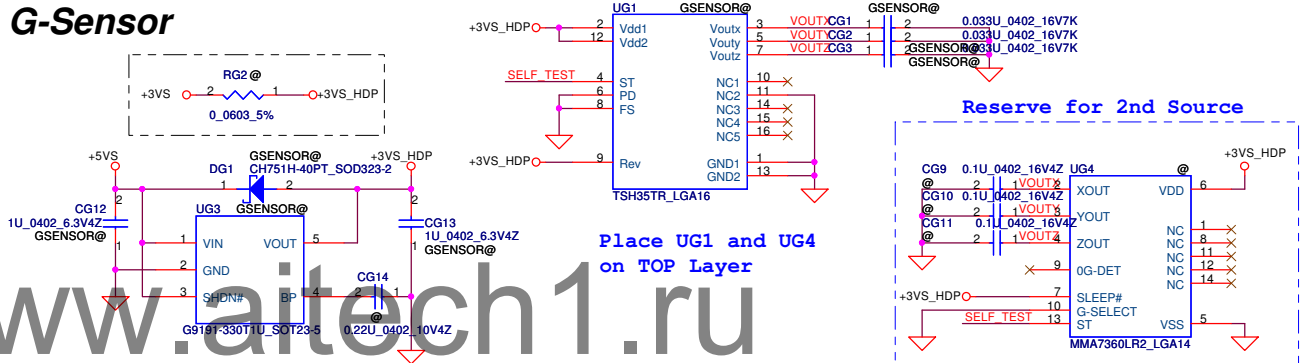
LPC Debug Port



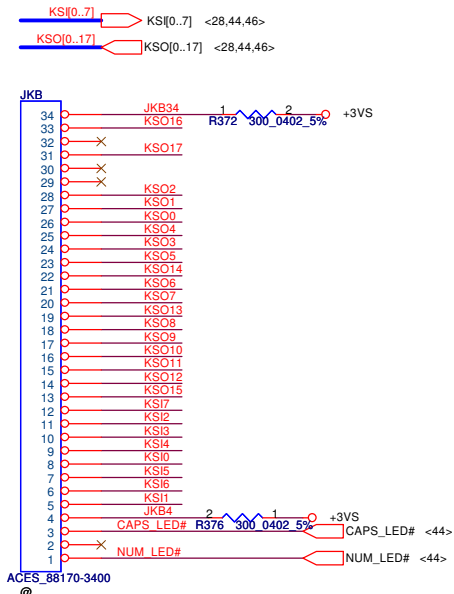
Keyboard LED



G-Sensor



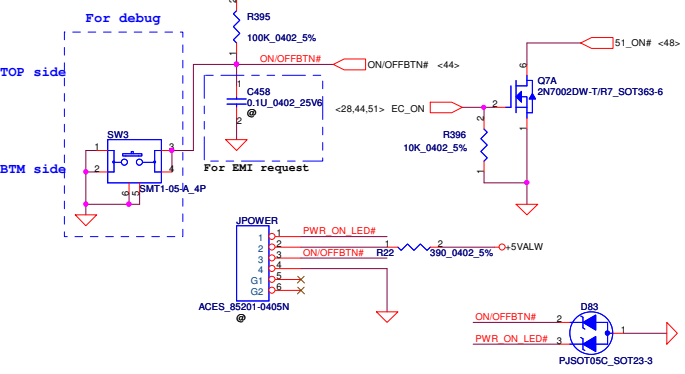
KEYBOARD CONN.



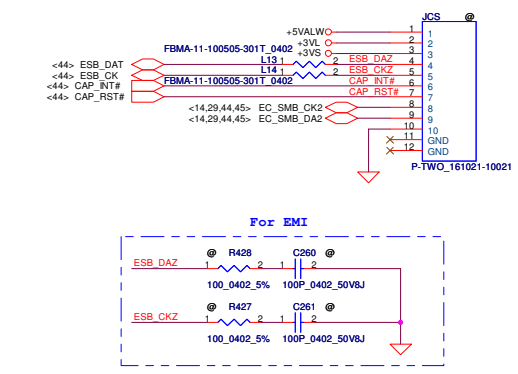
For EMI	Close to JKB
KSO16	C401
KSO17	C402
KSO2	C404
KSO1	C405
KSO4	C406
KSO3	C407
KSO5	C408
KSO6	C409
KSO7	C410
KSO13	C412
KSO8	C413
KSO9	C415
KSO10	C416
KSO11	C417
KSO12	C418
KSO15	C419
KSI7	C420
KSI2	C421
KSI3	C422
KSI4	C423
KSI0	C424
KSI5	C425
KSI6	C427
KSI1	C429
CAPS_LED#	C431
CAPS_LED#	C433
NUM_LED#	C435

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Issued Date	200910/9	Deciphered Date	2010/01/23	Title
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Size	Document Number	PHQAA LA-6831P M/B		Rev 0.1
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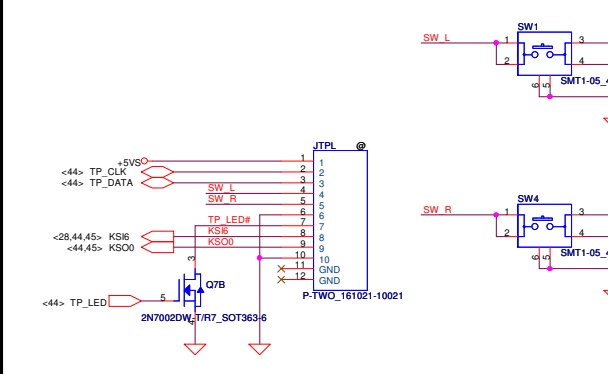
Power Button



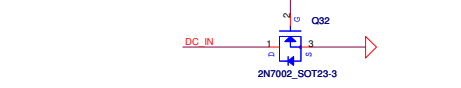
Caps Sensor/Light Sensor Conn.



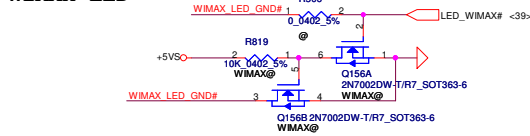
Touchpad & Light Pipe Connector



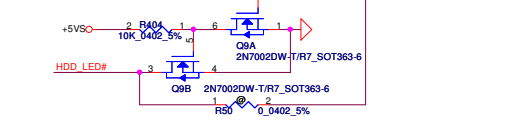
DC-IN LED



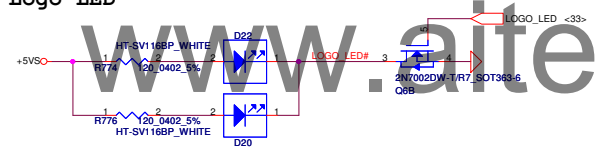
WiMAX LED



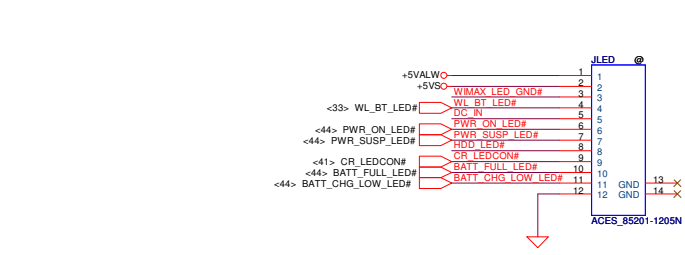
HDD LED



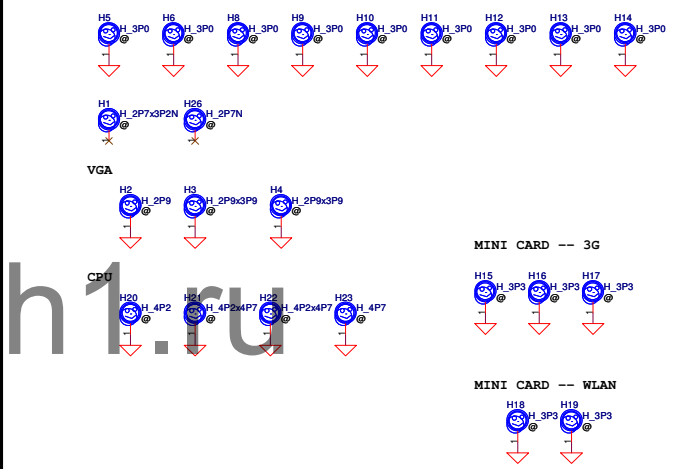
Logo LED



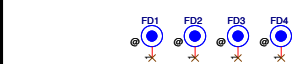
LED/B Connector



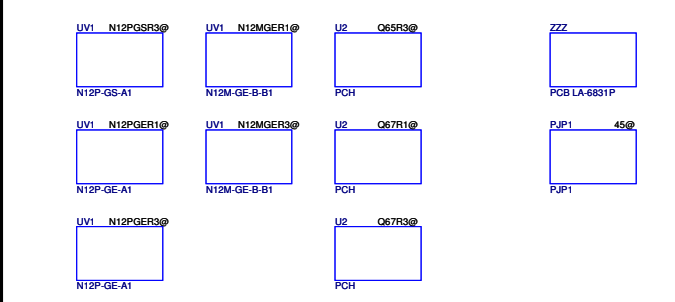
Screw Hole



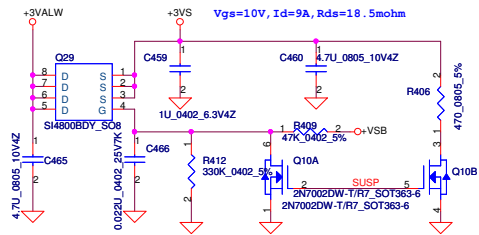
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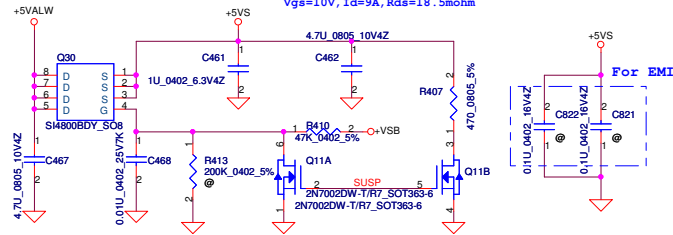
ISPD



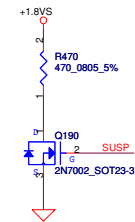
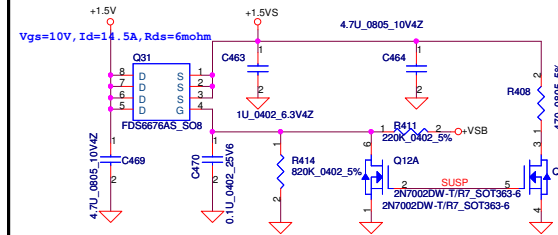
+3VALW TO +3VS



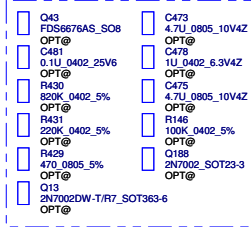
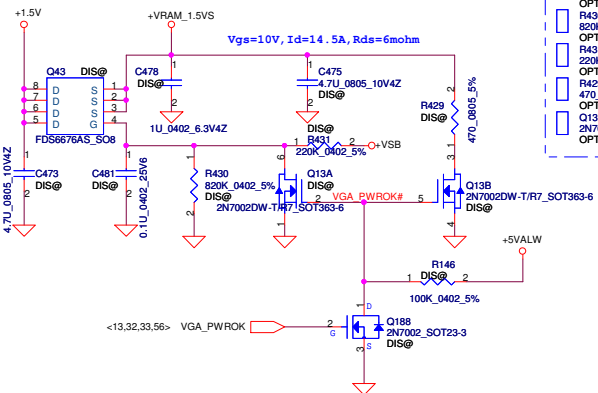
+5VALW TO +5VS



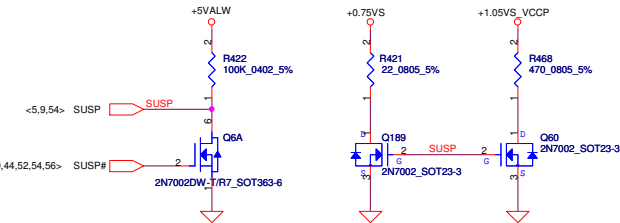
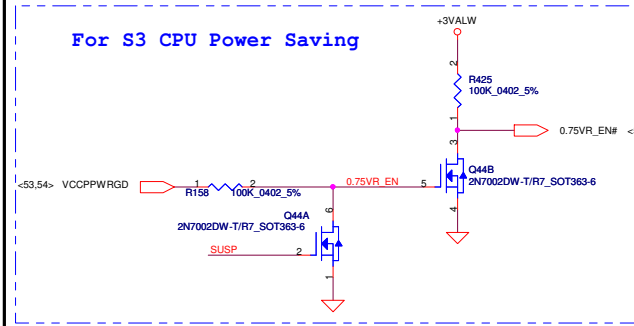
+1.5V to +1.5VS



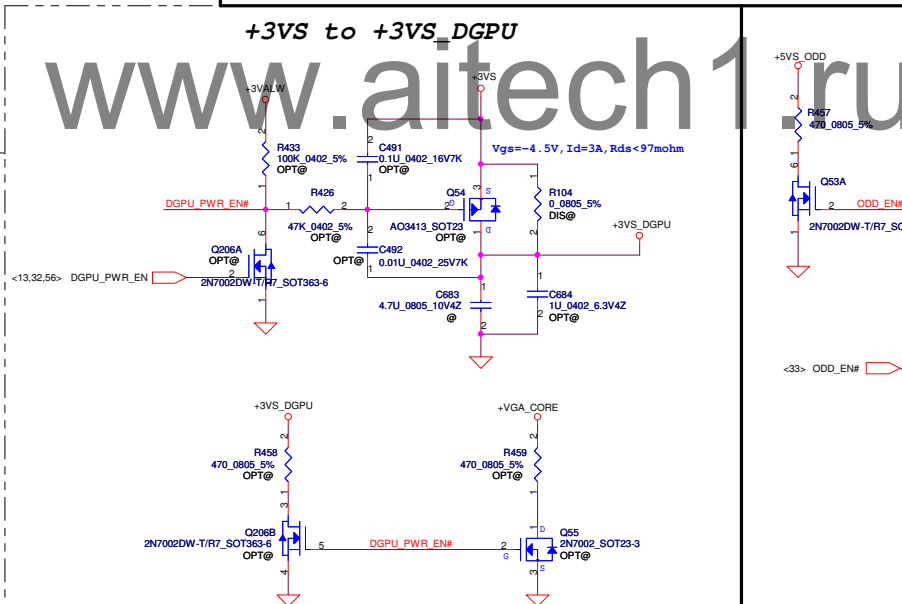
+1.5V to +VRAM_1.5VS



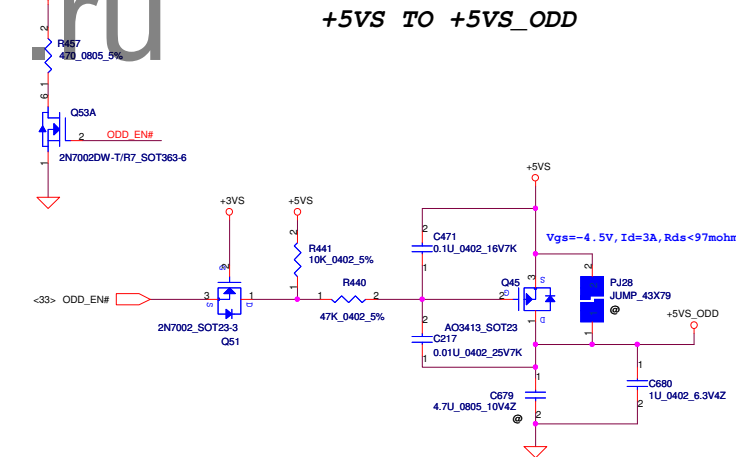
For S3 CPU Power Saving



+3VS to +3VS_DGPU

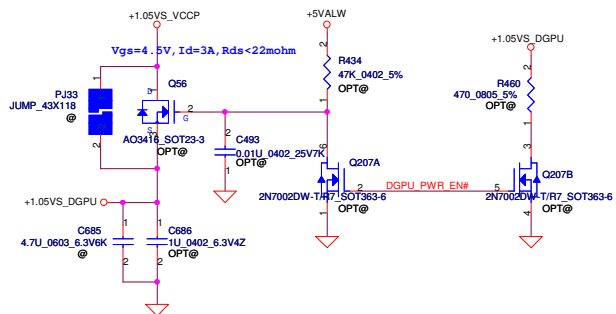


+5VS TO +5VS_ODD



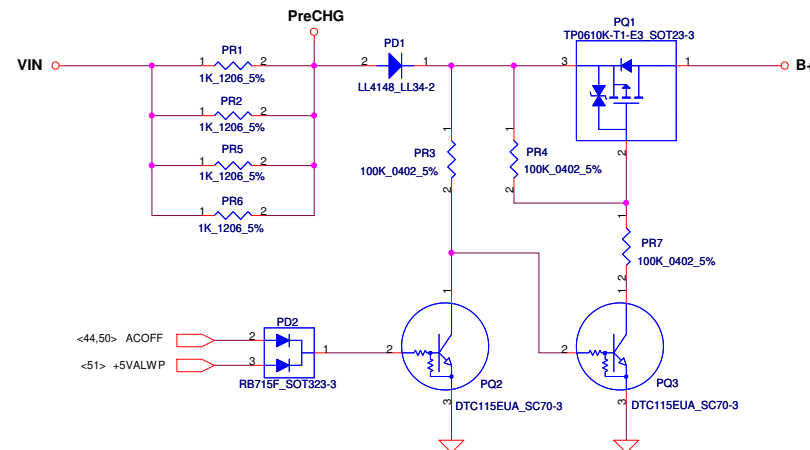
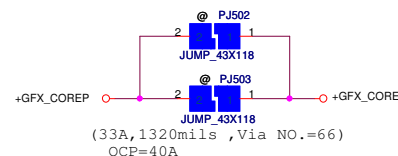
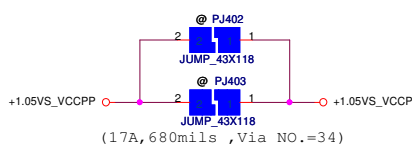
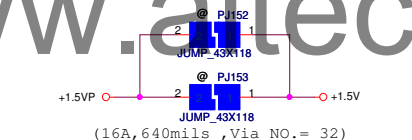
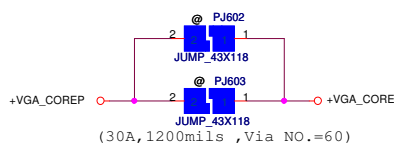
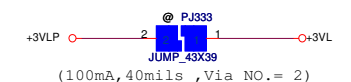
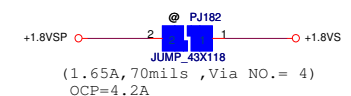
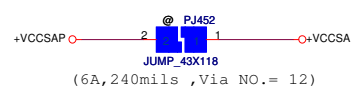
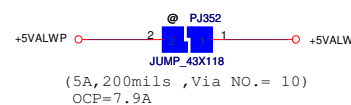
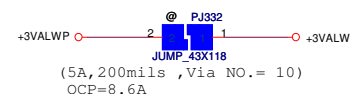
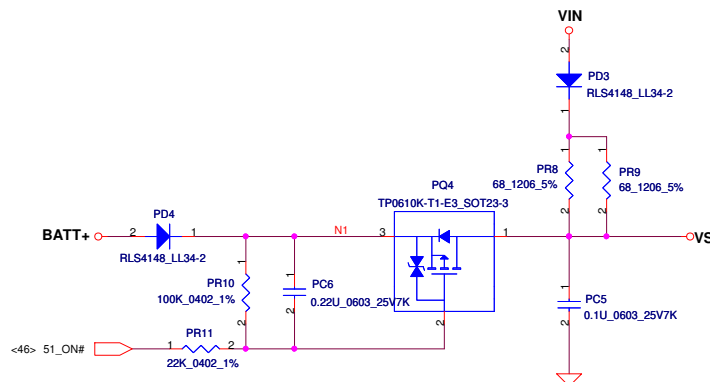
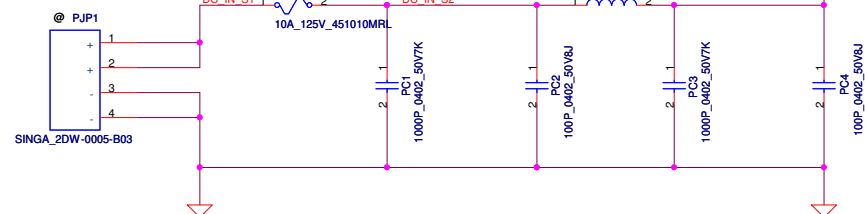
+1.05VS_VCCP to +1.05VS_DGPU

Short PJ33 for Discrete SKUs

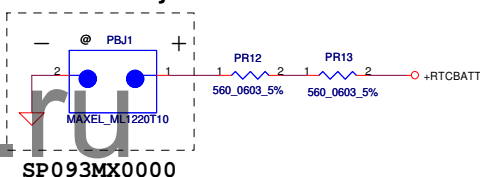


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				Size	Document Number
				PHQAA LA-6831P M/B	
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DC301001M80



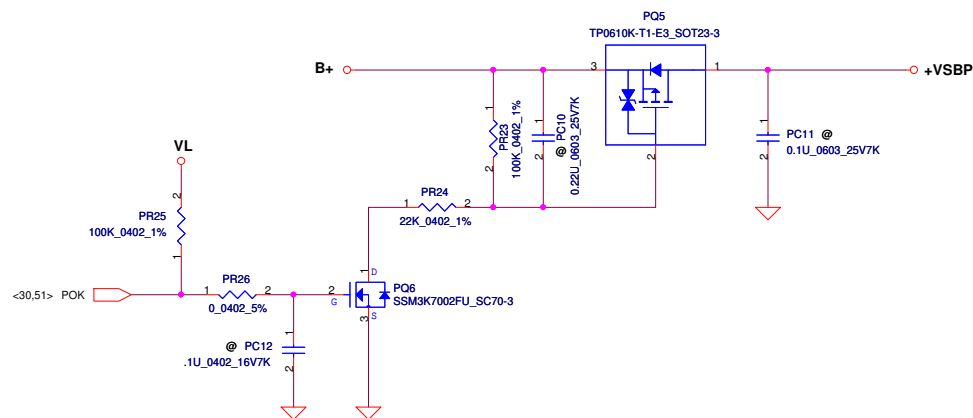
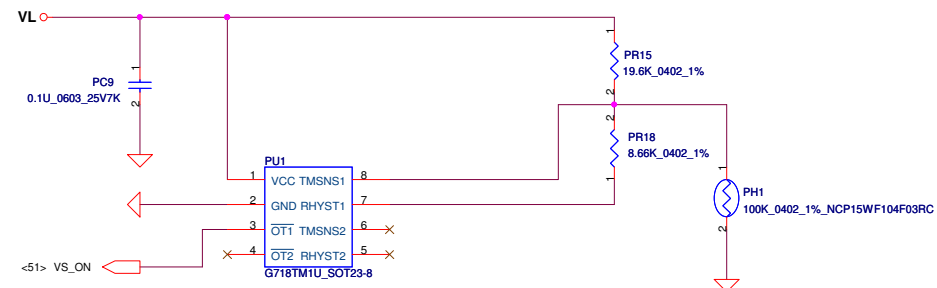
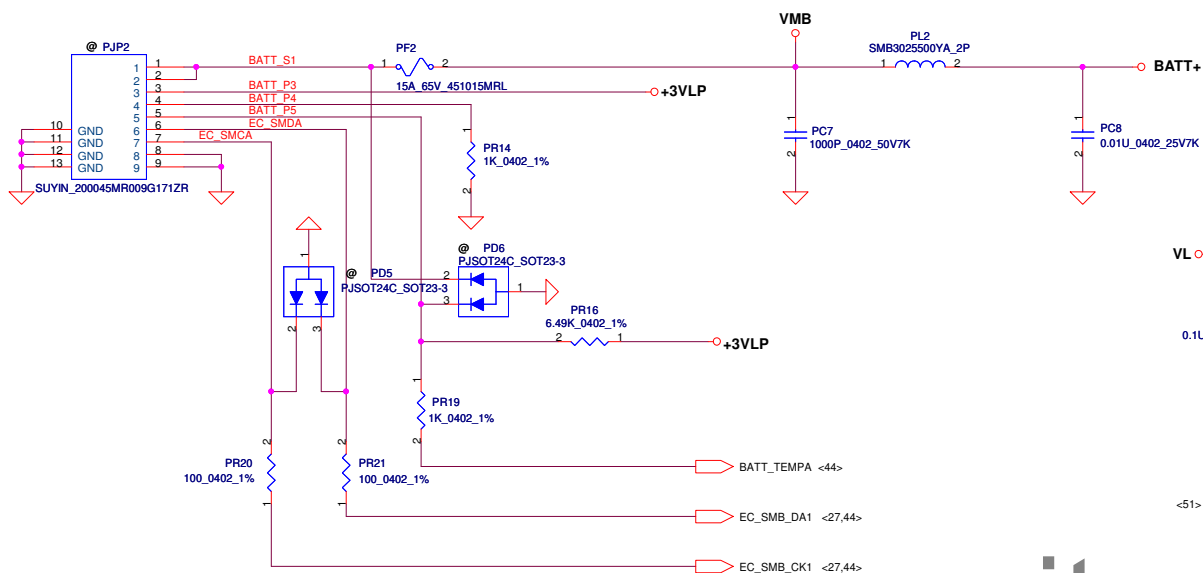
RTC Battery



ACIN

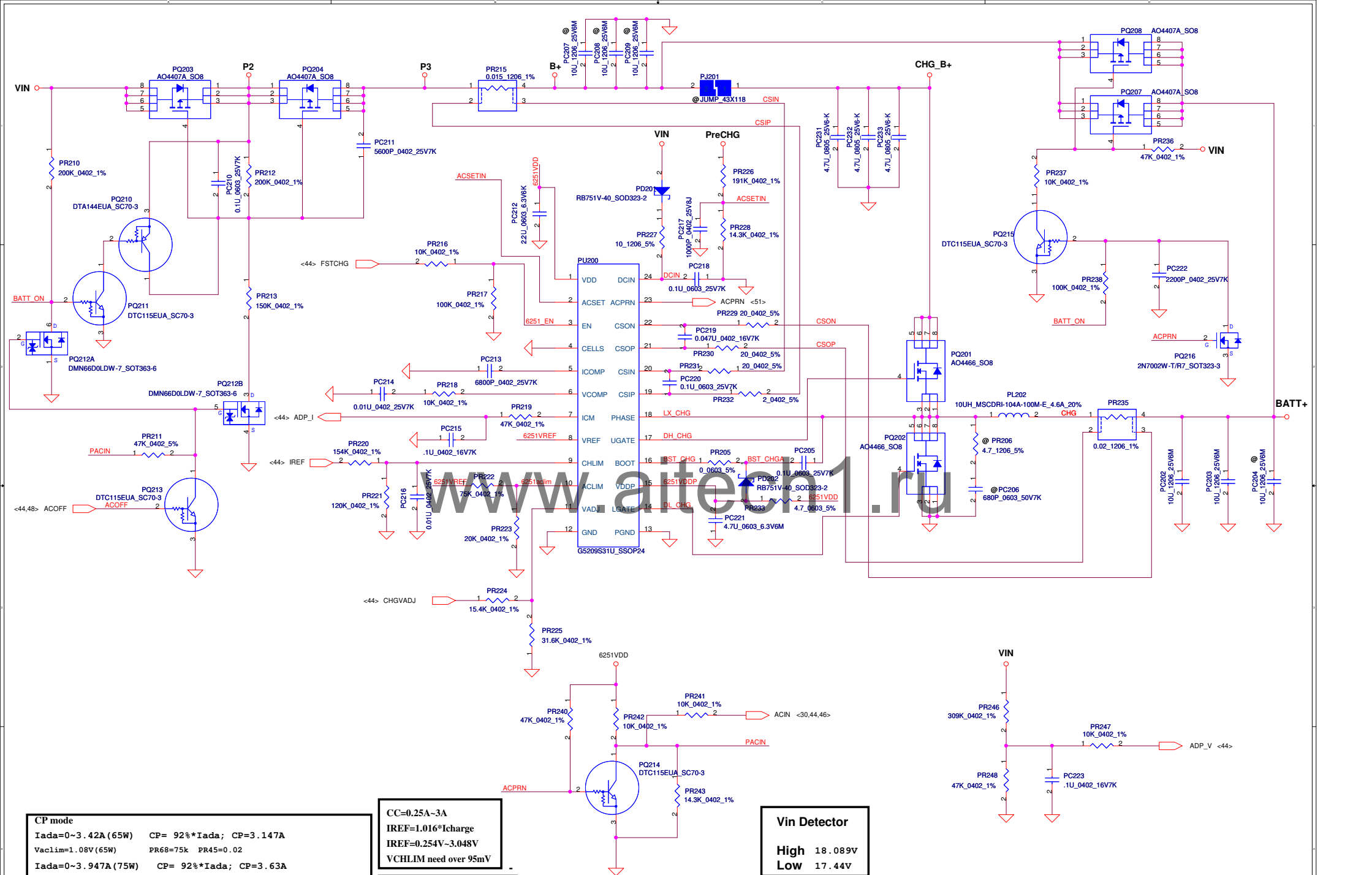
	Min.	typ.	Max.
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

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				Date:	Monday, August 02, 2010
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				Rev	0.1



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Issued Date				2009/11/13				Deciphered Date			
2009/04/28				Title				BATTERY CONN / OTP			
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				NHQAA LA-6831P M/B				Rev			
Date: Monday, August 02, 2010				Sheet				49 of 58			



CP mode

I_{ada}=0~3.42A (65W) CP= 92%*I_{ada}; CP=3.147A
 Vac_{lim}=1.08V (65W) PR68=75k PR45=0.02

I_{ada}=0~3.947A (75W) CP= 92%*I_{ada}; CP=3.63A
 Vac_{lim}=0.736V (75W) PR68=24k PR70=20k PR49=0.02

I_{ada}=0~4.737A (90W) CP= 92%*I_{ada}; CP=4.36A
 Vac_{lim}=0.736V (90W) PR68=53.6k PR70=20k PR49=0.015

I_{ada}=0~6.316A (120W) CP= 92%*I_{ada}; CP=5.81A
 Vac_{lim}=0.736V (120W) PR68=8.25k PR70=26.7k PR49=0.015

CC=0.25A~3A
 IREF=1.016*I_{charge}
 IREF=0.254V~3.048V
 VCHLIM need over 95mV

CHGVADJ=(V_{cell}-4)*9.445

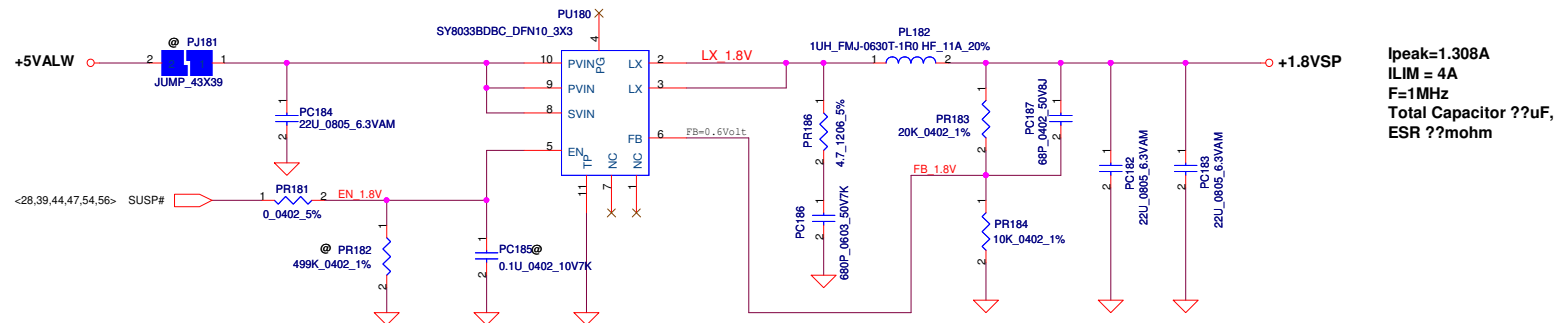
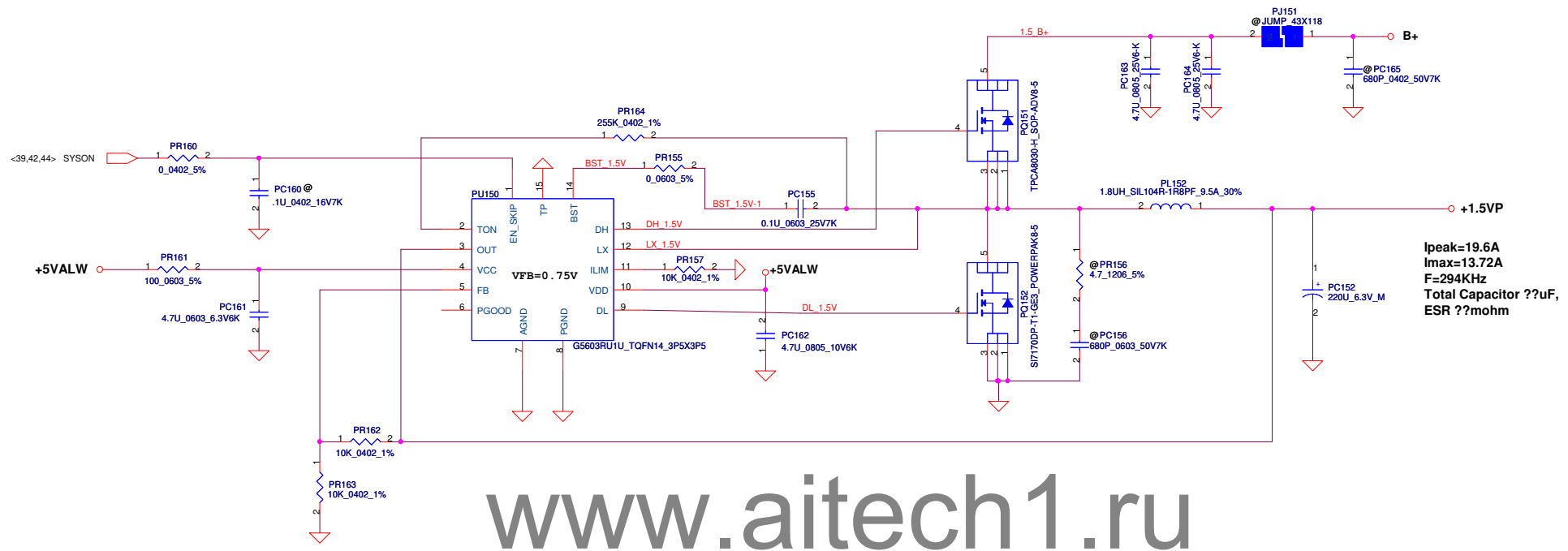
V _{cell}	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

Vin Detector

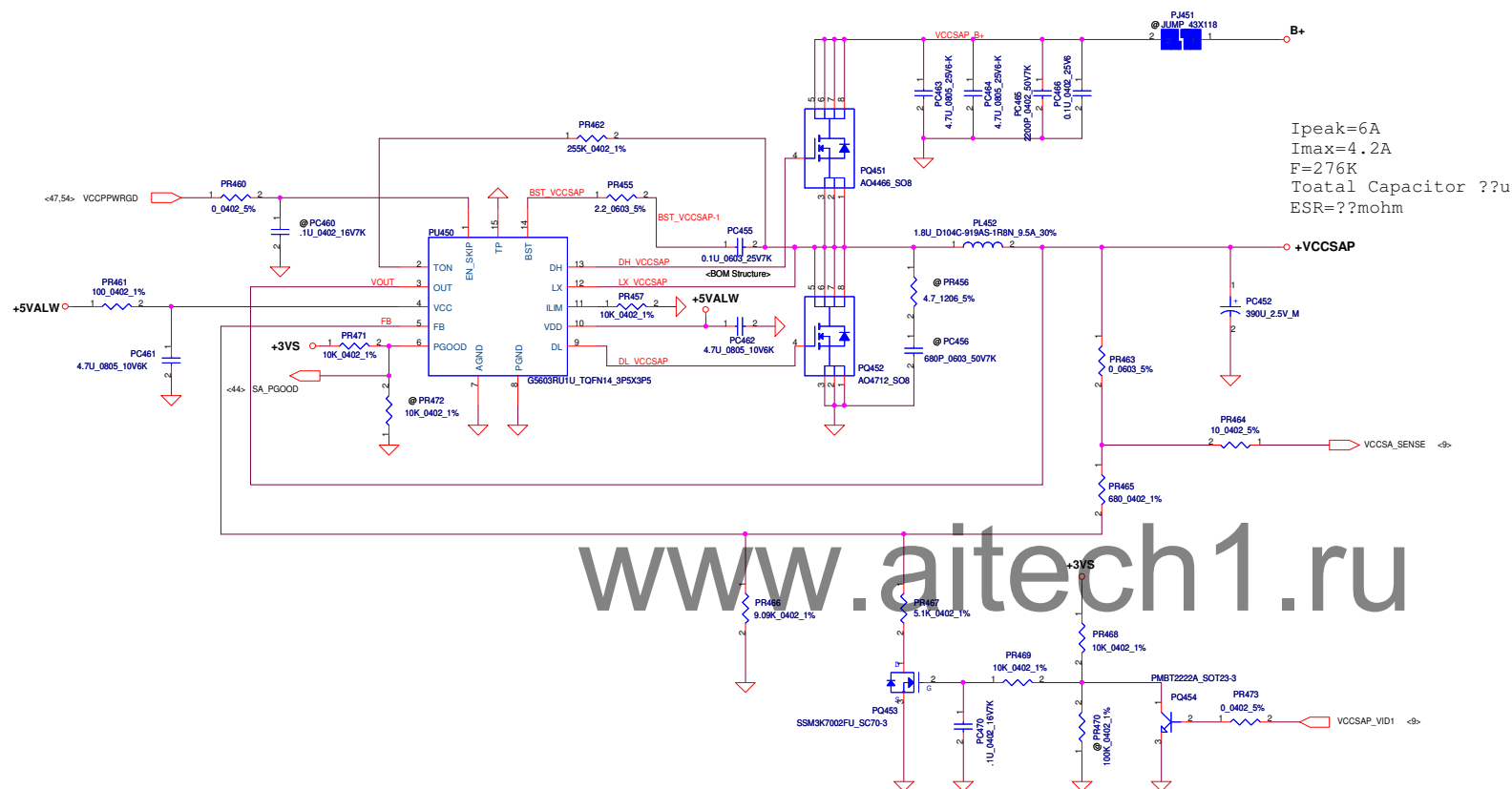
High 18.089V
 Low 17.44V

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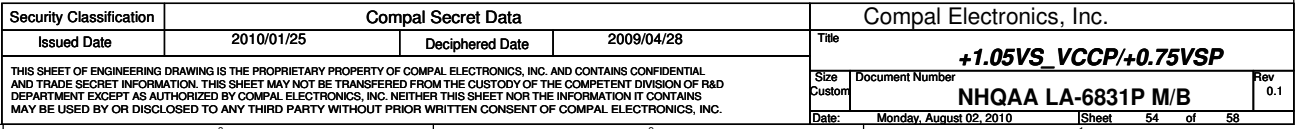


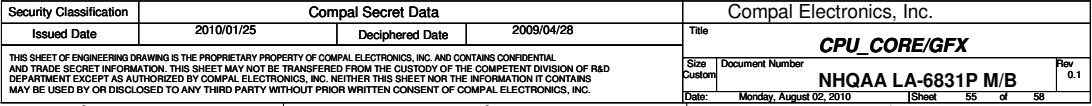
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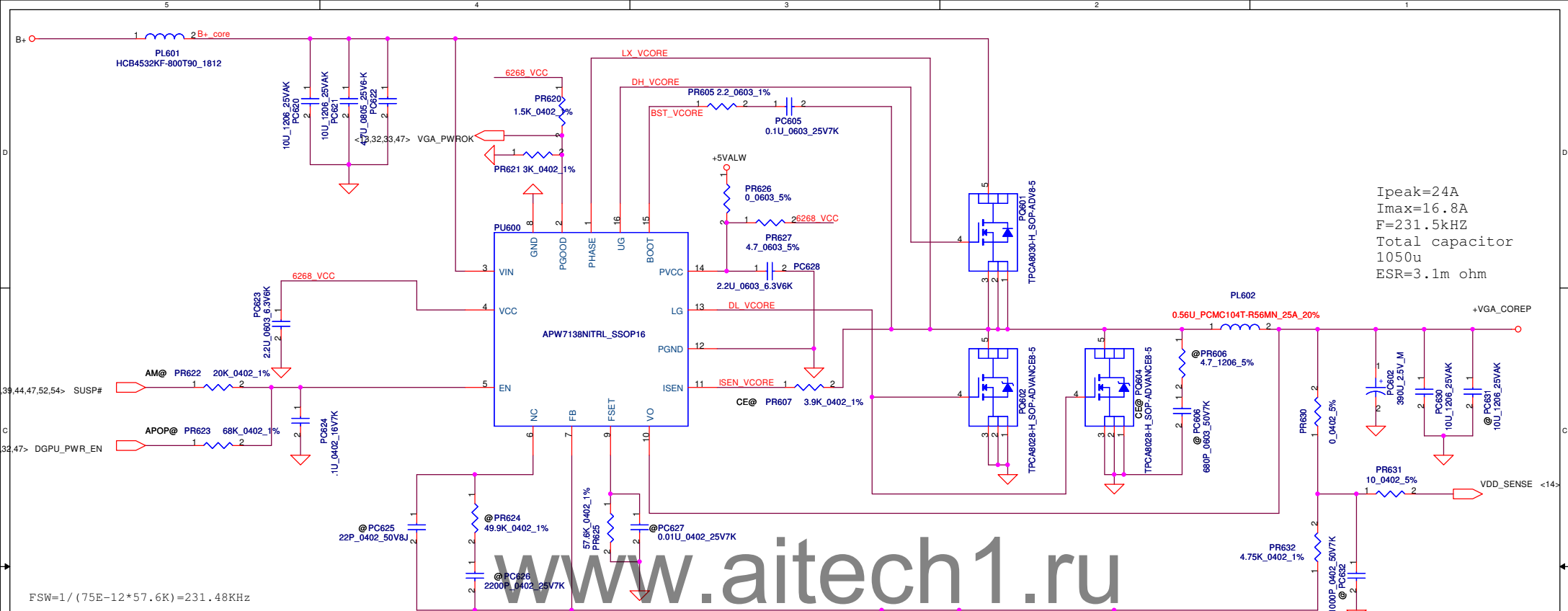


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VID1	+VCCSAP
1	0.8V
0	0.9V







N11M-GE1/GE2	N11P-GE1/GE2	N11E-GE1_LP
Imax=16.09A Ipeak=18.19A Iocp=20.72A	Imax=16.8A Ipeak=24A Iocp=29.17A	Imax=16.8A Ipeak=24A Iocp=32.14A
PR255=5.36K PQ50=unpop	PR255=7.15K PQ50=unpop	PR255=7.15K PQ50=unpop

$$VFB(0.6) = V_{out} \cdot R_{bottom} / (R_{top} + R_{bottom})$$

GPU_VID0	GPU_VID1	N11M-GE1	N11M-GE2	N11P-GE1	N11P-GE2	N11E-GE1-LP
0	0			0.80V	0.80V	0.80V
1	0	0.85V	0.85V	0.85V	0.85V	0.85V
0	1					
1	1	1.03V	1V	0.95V	0.925V	0.9V
		PR260=4.75K PR262=14K PR261=56.2K PR263=16.2K	PR260=4.75K PR262=14K PR261=56.2K PR263=19.6K	PR260=4.75K PR262=14K PR261=56.2K PR263=29.4K	PR260=4.75K PR262=14K PR261=56.2K PR263=40.2K	PR260=4.75K PR262=14K PR261=56.2K PR263=63.4K

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HW PIR (Product Improve Record)

NWQAA LA-6062P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2
GERBER-OUT DATE: 2009/12/30
NO DATE PAGE MODIFICATION LIST

PURPOSE

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2010/04/20	P36-P45	Release	

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